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Effect of temperature and film thickness on resistivity of CoWP

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Introduction:

There is recent interest in using Co alloys, such as CoWP, as a capping layer on top of Cu interconnects [1, 2, 3]. The advantages of using CoWP as a capping layer, rather than conventional dielectric capping layers, include improved electromigration for microprocessors [4] and the elimination of reflecting layers in the optical path for CMOS image sensors [1]. The resistivity of CoWP capping layers is important for a number of reasons. First, if CoWP is left at the bottom of the via , the via resistance is increased due to the higher resistivity of the Co alloy [1,2]. In addition, during an electromigration stress, the Co alloy may shunt current around a void, if the resistivity is sufficiently low.

The resistivity of Co alloys deposited by electroless deposition is difficult to measure for the thicknesses (<50 nm) and the substrates (Cu) of interest for microelectronics, due to the low resistivity of the underlying Cu. Most of the data in the literature is for very thick films (100 nm or greater) without annealing. The reported resistivities vary widely, ranging from 41 μΩ-cm for CoWP to 282 μΩ-cm for CoWB [5,6]. There is little data on how the resistivity varies with temperature. In this study, CoWP films are deposited on SiO_2 substrates, and the resistivity is characterized as a function of thickness, annealing, and temperature.

Results and Discussion:

The via chain resistance is higher for samples with CoWP capping layers (Fig. 1) compared to those without, due to the additional resistance associated with CoWP at the bottom of the via. For the 40 nm CoWP sample, the via resistance is higher than the control sample by 0.4 Ω. The thickness of CoWP remaining at the bottom of the via is 15 nm (Fig. 2), corresponding to a resistivity of 35 μΩ-cm.

The room temperature resistivity (Fig. 3) is strongly dependent on film thickness and annealing conditions. The resistivity rapidly increases for film thicknesses below 50 nm. However, the film resistivity decreases dramatically with annealing. The variation in resistance as a function of measurement temperature is strongly dependent on the anneal conditions (Fig. 4). Unannealed films show almost no change in resistance with measurement temperature, suggesting that impurity scattering dominates. However, the resistivity of annealed films increases with measurement temperature, consistent with phonon scattering.

The resistivity data suggests that in the as-deposited films, the W and P are uniformly distributed throughout the Co grains. However, after annealing, these dopants and other impurities segregate to the Co grain boundaries, resulting in reduced impurity scattering.

The film thicknesses measured by the weight gain method and RBS are generally in good agreement (Fig. 5). The CoWP composition appears to be slightly dependent on thickness, with higher P concentrations as film thickness decreases. The CoWP composition is close to that used in previous reports on integrated structures [4]. Cross-section TEM images (Fig. 6) show that all the films are polycrystalline, with considerable surface roughness. Images from 30 nm films (Fig. 6a and 6b) indicate that the roughness increases after annealing. The grain size is approximately equal to the film thickness for all films. High resolution images of the 300°C annealed samples shows lattice planes, confirming the films are polycrystalline (Fig. 7). X-ray diffraction data from the 400°C annealed films show peaks, corresponding to the hcp phase of Co .

Finally, the CoWP resistivity determined from the via chain resistance is much lower than that determined from four point probe measurements on blanket films (i.e., even with a 400°C anneal, the 40 nm blanket CoWP films have a resistivity of almost 100 μΩ-cm). A possible reason for the difference is that for vertical conduction (through vias) the current does not have to traverse grain boundaries in the CoWP, whereas for lateral conduction (blanket films), current must traverse grain boundaries, resulting in higher measured resistivity.

Conclusion:

In this study, CoWP films are deposited on SiO_2 substrates, and the resistivity is characterized as a function of thickness, annealing, and temperature. Unannealed films show almost no change in resistance with measurement temperature, suggesting that impurity scattering dominates. In contrast, annealed films show an increase in resistivity with temperature, consistent with phonon scattering. It is proposed that dopants and impurities segregate to Co grain boundaries during annealing, resulting in a large reduction in resistivity. The CoWP resistivity determined from the via chain

resistance is much lower than that determined from four point probe measurements on blanket films, probably due to less grain boundary scattering for vertical current flow compared to lateral current flow.

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3. E.J. O'Sullivan et al., IBM J. Res. Dev., **42**, 607 (1998).
4. C.-K. Hu et al., Microelec. Eng., **70**, 406 (2003).
5. A. Kohn et al., Mater. Sci. Eng. A, **302**, 18 (2001).
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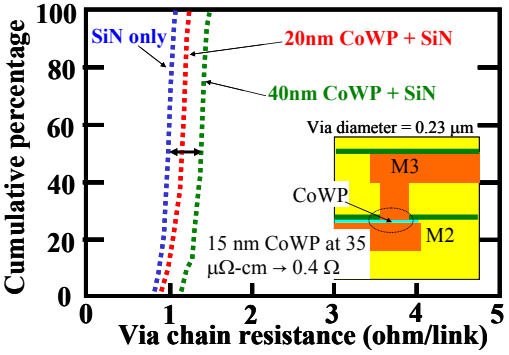

Fig. 1. Via chain resistance

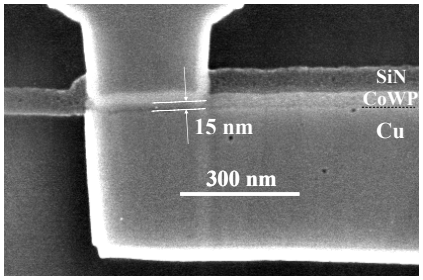

Fig. 2. SEM of CoWP in bottom of via.

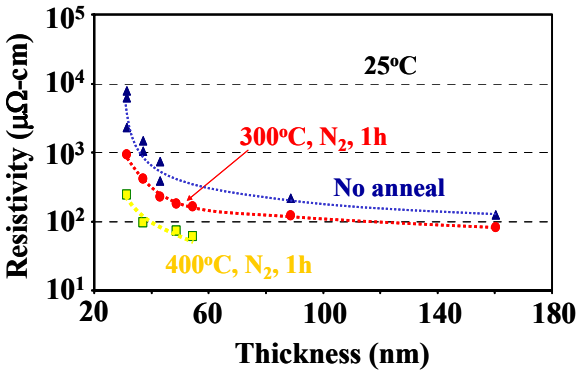

Fig. 3. Resistivity of CoWP on SiO_2.

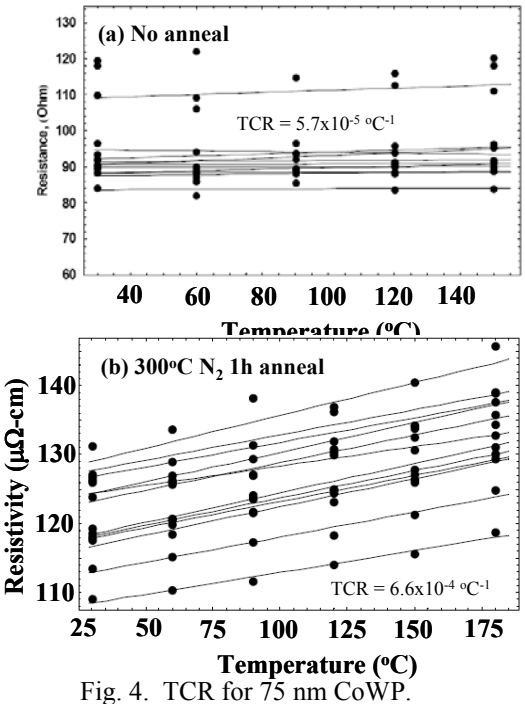

Fig. 4. TCR for 75 nm CoWP.

measured thickness wt gain (nm)	measured thickness RBS (nm)	composition		
		Co atm %	W atm %	P atm %
31	30	91	1	8
43	34	92	1	7
89	75	93	1	6
160	145	95	1	4

Fig. 5. CoWP composition and thickness.

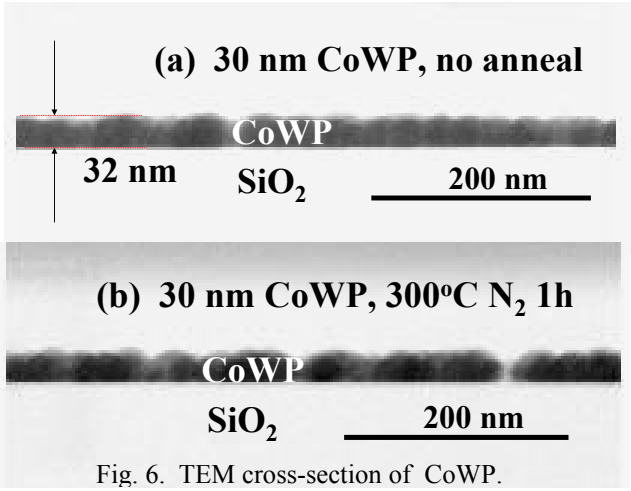

Fig. 6. TEM cross-section of CoWP.

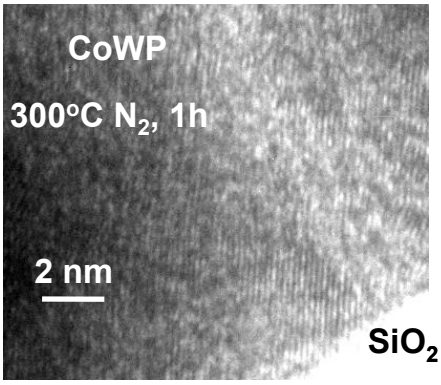

Fig. 7. TEM lattice fringe image of CoWP.