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Low-k/Cu Integration Consistent from 90nm thru 32nm (invited)

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1. Introduction

While a variety of integration schemes and new process modules/materials have been investigated for low-k/copper integration, IBM has been extending the simplest integration scheme from the 90 nm PECVD Low-k/Cu Integration to the 45 nm porous low-k/Cu integration and beyond. This simplest scheme has been supported mainly by the in-house designed low-k materials and the direct CMP. In this talk, these essential features of our low-k/copper integration scheme consistent to all technical nodes from 90 nm to 45 nm are reviewed with some other key features vital to its high level reliability.

2. Monolithic PECVD Low-k/Cu Dual Damascene

Since our inception of Cu in 1997 [1], IBM has been extending the simplest dual damascene scheme. Fig. 1 illustrates the monolithic PECVD Low-k/Cu Dual Damascene scheme consistently developed and applied throughout the technical nodes [1-6]. No etching stop and no hard mask retention have been applied from the inception of Cu. The PECVD SiCOH/Cu integration started from the 90 nm node [2-6]. The simplest does not always mean the easiest. There are number of technical challenges that we needed to work out. Trench/via pattern definition by RIE is one of the largest difficulties that we have overcome. Since there is no etching stopper or etching selectivity between the trench and via level low-k materials, the RIE conditions were optimized so that variety of patterns on a wafer can be defined correctly.

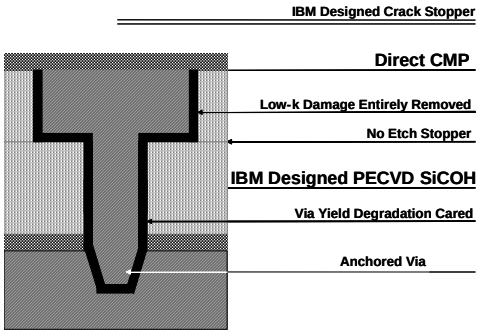

Figure 1 IBM's Monolithic SiCOH Low-k/Cu Integration

It has been proven through the development work that the modern plasma etchers do the work as required [4]. Via Yield Degradation has been used as the monitor for optimization of the process conditions and to examine the healthiness of the integrated process flow [3]. Another challenge we have gone through is the direct CMP of the low-k material [7]. The direct CMP has been the indispensable process module for us to stay with the simplest monolithic damascene scheme which does not have the hard mask left on top of the low-k dielectrics (See Fig. 1). By the successful adoption of the direct CMP, the lowest possible effective interconnect capacitance has been achieved as depicted in Fig. 2. In other words, it allows the strongest ILD at higher k to be applied for the metal system to get the same final k_{eff}, or in turn to get the lowest k_{eff} for the same ILD, which is crucially important because process difficulties exponentially and monotonically increase as dielectric materials used in the integration become lower-k with regards to RIE, wet

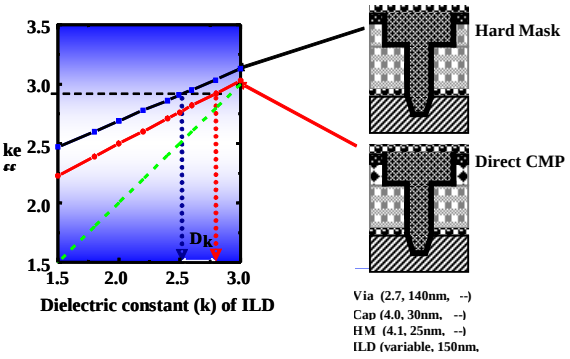

Figure 2 Effective k-values in Hard Mask Retention and Direct CMP Schemes [8]

cleaning, dicing and packaging, and the direct CMP [8]. Leaving no hard mask by direct CMP is beneficial also for the ventilation to dry the ILD prior to the cap deposition. Also, other difficulties arising by the retention of the hard mask during CMP are hard mask erosion and breaching defects due to across-the-wafer non-uniformity of CMP. The plasma damage onto the low-k ILD which has a potential cause for reliability problems such as TDDB is common to both schemes and therefore, makes no difference between the two schemes. Table-I lists the pro and con of the two schemes.

Table-I Direct CMP and Hard Mask Retention Schemes

	Pro	Con	Even
Direct CMP	i) Lowest Possible k-eff ii) No Notched Trench iii) Less worry about CMP Non-Uniformity	CMP damage on top of Low-k i) CMP Non-Uniformity ii) Notched Trench Entrance iii) Higher k-eff	Plasma Damage on top of Low-k
Hard Mask Retention	Organic Low-k is applicable to Trench Level		

3. Direct CMP and Originally Developed Low-k

The monolithic PECVD Low-k/Cu scheme has been supported and extended by the direct CMP technology and the home-made PECVD low-k and ultra low-k SiCOH materials [8, 9]. Direct CMP is apt to cause so-called CMP damage on the SiCOH materials especially when the low-k material is porous. As is shown in Fig. 3, some commercially available porous low-k material whose initial dielectric constant (k-value) is 2.3 has the resultant k-value of over 5 after the direct CMP.

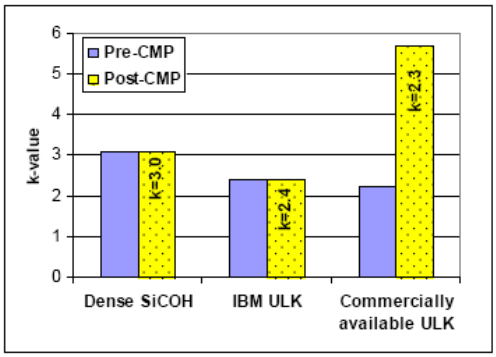

Figure 3 Effects of Direct CMP on k-value [10]

On the contrary, the porous low-k dielectric developed originally in IBM does not change its k-value even after the direct CMP (Fig. 3). This remarkable performance is one of the major enablers which let us stay with the monolithic damascene scheme even in the 45 nm node. The eCMP which has a high capability for planarization and enables the low CMP down force is another contributor to this success [7]. Fig. 4 shows the FT-IR spectra for the home-made porous SiCOH before and after the UV curing. The Si-CH3 absorbance at 1275cm^{-1}

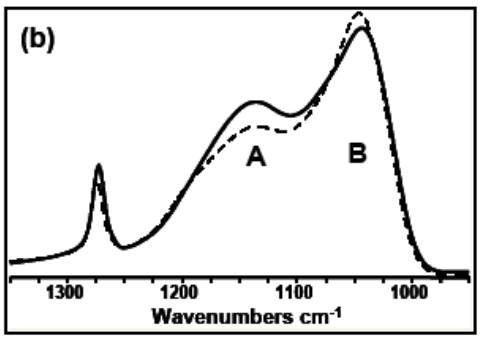

Figure 4 FT-IR spectra of as deposited (solid) and UV cured (dashed) IBM porous SiCOH films [10]

does not change so much after the UV curing. Comparison of the integrated FT-IR spectra at the peak revealed that the IBM porous low-k film has 80% higher Si-CH3 bonding in the film. Such a high Si-CH3 content in the film gives the film high hydrophobicity which, together with its isolated pore structure [10], does not allow any hydrous components to intrude into the porous low-k film supporting us to apply the direct CMP.

4. Other Key Features of IBM's Low-k/Cu Scheme

The gouged via structure since the 130 nm node gives the high level reliability such as EM and SM to our low-k/Cu chips. PECVD low-k integration in the 90 nm node started by using the k=3.0 home-made PECVD low-k film named Gen-III [11, 12] which has a remarkably high immunity against crack and crack propagation [12]. Although the mechanical strength of low-k ILD films gradually lowers for the lower k, reengineered crack-stop, optimized dicing technology, and the strongest ILD adhesion have allowed CPI passing with standard underfill materials which have been vital to production of low-k/Cu IBM chips [12, 13].

5. Air Gap Technology

Several research institutes have published Air Gap technologies including IBM [14-18]. Air Gap can reduce interconnect capacitance dramatically. However, there are number of technical issues to be worked out such as miss-alignment of via landing to the underlying metal layer, how to reduce the extra production cost associated with additional lithography steps, and how to remain or recover the planarity after air gap formation. Use of an additional lithography to exclude via landing areas named as Air Gap Exclusion seems a promising approach to the miss-alignment problem [16]. Several approaches for Air Gap formation such as the non-conformal CVD pinch-off and the sacrificial ILD may be categorized into two. One is "Add-on" approach to the existing BEOL flow and the other is a totally new approach with the Air Gap specified process flow. Air Gap is no doubt one of the promising future technologies.

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