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Next generation compact model for digital and analog circuit design

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I. Introduction

The trend of compact model development for bulk CMOS leads to models based on surface potential, allowing higher accuracy in comparison to the threshold voltage based models [1, 2]. The main reason for high accuracy is that the surface potential model is suitable for the description of device physics than Vth and inversion charged model. High speed simulation run-time and good convergence are required to next generation compact model because the transistor number for circuits has been increasing with progress of technology node. Additionally, quick way to extract parameter is also required because the many kinds of MOSFETs with multi Vth and multi supply voltage are needed for circuit design. In this paper, benchmark results about digital, analog circuits and parameter extraction are shown.

II New concept of next generation compact model

Table I shows types of MOSFET compact model. In Vth based model such as BSIM3 and 4, drift and diffusion current model are connected around Vth by using smoothing function. This model is sufficient for digital circuit design because standby current and drivability is mainly important to simulate operation speed and power consumption. However, the accuracy around Vth is not sufficient for analog and RF design because high order derivatives characteristics are important for the design. In new model, those are considered in all operation regions. The newest concept is surface potential model such as PSP and HiSIM. HiSIM solves the surface potential ϕ_s with the iteration procedure, while PSP calculate ϕ_s with simplified analytical equation [3]. The any computer run-time penalty by iteration can be neglected because the number is small because an initial value before iterative calculation is high accuracy as shown in fig1.

III Benchmark results

Fig.2 shows procedure for parameter extraction in BSIM4, PSP and HiSIM. In both BSIM4 and HiSIM, one parameter set is extracted in order to fit with all measurement data. On the other hand, 2 steps extraction has been needed in PSP model. The parameter for global model is extracted based on many local model parameter sets extracted from each geometry MOSFET data. This procedure is more complex than BSIM4 and HiSIM case. Fig.3 shows gummel symmetry test for Ids up to 3rd derivative in 90nm technology CMOS for PSP and HiSIM. Simulation and measurement results are plotted. In this test, Vx and –Vx was applied to drain and source, respectively. The source-drain symmetry of MOSFETs is important when the operating point of MOSFETs swing passes through Vds = 0V [4]. In both models, the simulation results were good agreement with measurement results. Additionally, IM3 was simulated by test circuit as shown in fig.4 in order to evaluate symmetry effect when Vds = 0V. In this circuit, power (Pin) of from -10 to 0dBm with 3.5 and 4.5 MHz were inputted to source and drain concurrently. The amplitude of output signal with 3.5 and 4.5MHz at drain is no distortion signal Po and that with 2.5 or 5.5MHz is IM3 signal. The slope in Po-Pin was 1 in all models, which is in perfect agreement with the theory. However the slope of IM3-Pin in BSIM4 was 2, which is in large disagreement. On the other hand, that was 2.7 in PSP and that was 3 in HiSIM, which is perfect agreement with the theory as shown in fig.5.

Fig.6 shows the evaluation results of 1/f noise model for BSIM4 and HiSIM. That for PSP model has not been evaluated yet. Used devices were 180nm technology NMOS. 1/f noise fitting were good in both models for NMOS with Lg of from 1μm to 0.2μm because the model has scalability as well as model for I-V characteristics. HiSIM model is more suitable than BSIM model for analog circuit design according to good symmetrical test, IM3 and 1/f noise results.

Fig.7 shows configuration of our high-density SRAM (HD-SRAM) cell for evaluation of simulation run-time and convergence. The number of nodes and elements in the circuit are 11,973 and 24,145, respectively. Three kinds of EDA vendor tools were used to simulate HD-SRAM. Simulated signal wave were same in all EDA vendor tools as shown in fig.7. Table II shows the run-time comparison, which is normalized by BSIM4 case. The results depend on the tool but it is clear that the run-time of PSP is the slowest among three compact models while BSIM4 is the fastest. The run-time of HiSIM is comparable with BSIM4 in an EDA tool. In any other test circuits such as comparator and operation Amp, no convergences of PSP were observed. At this stage, BSIM4 is the most suitable model for digital circuit design according to simulation run-time and convergence results. HiSIM has potential to catch up simulation run-time of BSIM4 model in near future. Table III shows the summary of our benchmark results. HiSIM will be useful for not only analog but also digital circuits design with improving of simulation run-time.

IV Conclusions

HiSIM model is more suitable than BSIM model for analog circuit design according to good symmetrical test, IM3 and 1/f noise results. PSP has the slower run-time and worse convergence problem. HiSIM will be useful for not only analog but also digital circuits design with improving of simulation run-time.

V References

[1] M. Miura et al., ED 2006, vol.53, No.9, pp.1994
[2] G. Gildenblat et al., ED 2006, vol53, No.9, pp.1979
[3] J. He et al., ED 2006, vol53, No.9, pp.2008
[4] C.C. McAndrew, ED 2006, vol53, No.9, pp.2202

Table I Types of MOSFET model

Vth model (1st generation)	BSIM3, BSIM4
Q_I model (2nd generation)	EKV, ACM, BSIM5
Φs model (3rd generation)	HiSIM, PSP

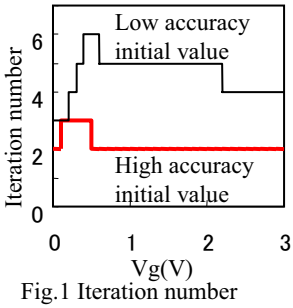

Fig.1 Iteration number for ϕs calculation in HiSIM

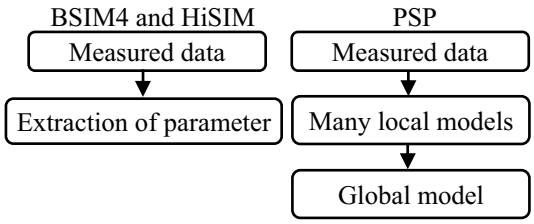

Fig.2 Procedure for parameter extraction in BSIM4, PSP and HiSIM. In PSP model, global model is formed based on local model extracted from each geometry MOSFET

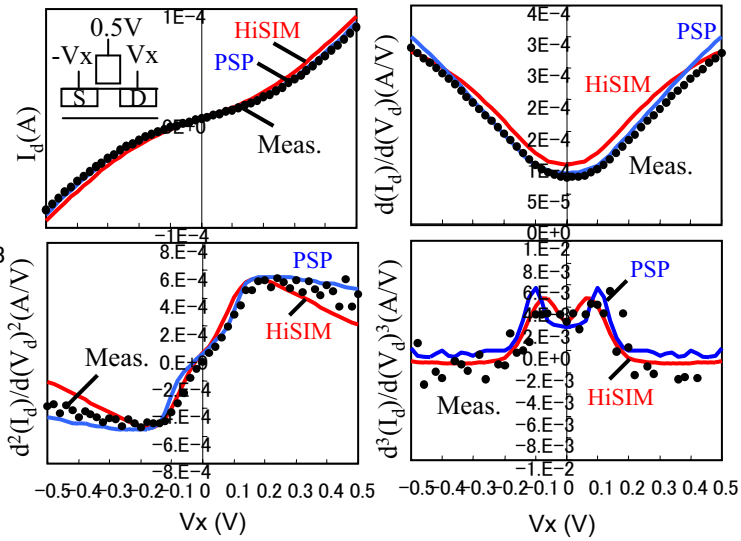

Fig.3 Gummel symmetry test for Ids up to the 3rd derivative for PSP and HiSIM. Comparison of simulation and measurements. Lg and Wg of the nMOSFET are 10μm and 10μm, respectively

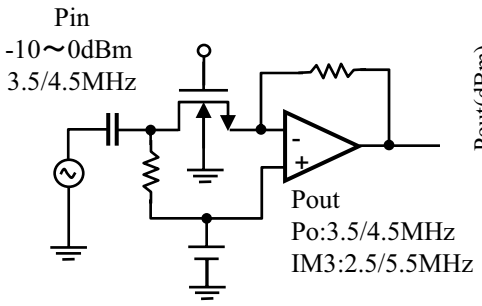

Fig.4 Circuit configuration for Pout and IM3 evaluation. 3.5 and 4.5 MHz are used for input signal frequency.

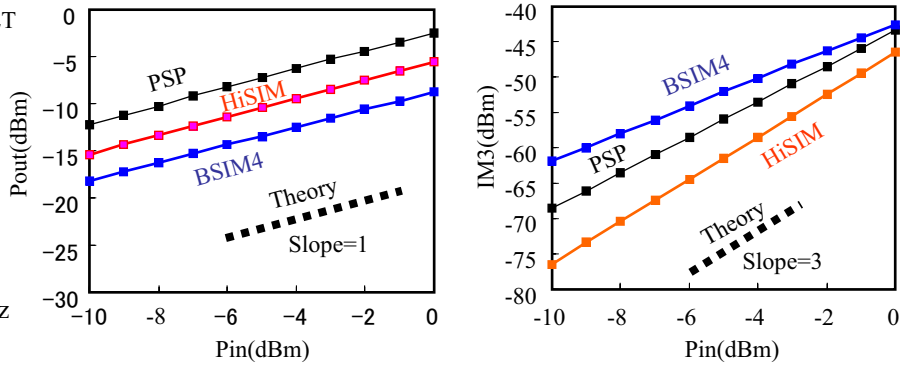

Fig.5 Pout and IM3 results for BSIM4, PSP and HiSIM. Slope in Pout is 1 in all models. In HiSIM model, the slope of IM3 is 3 which is perfect agreement with the theory.

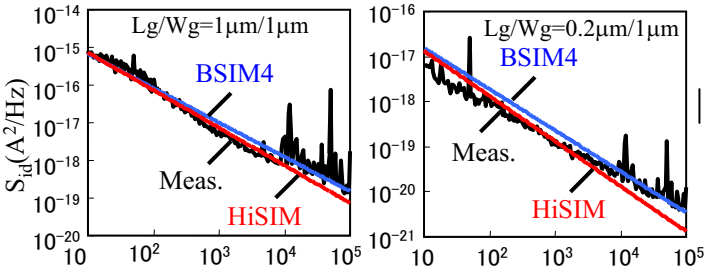

Fig.6 Comparison results of 1/f noise in BSIM4 and HiSIM. Used device are 180nm technology NMOS. Vd and Vg is 1.2V and Vth+0.6V, respectively.

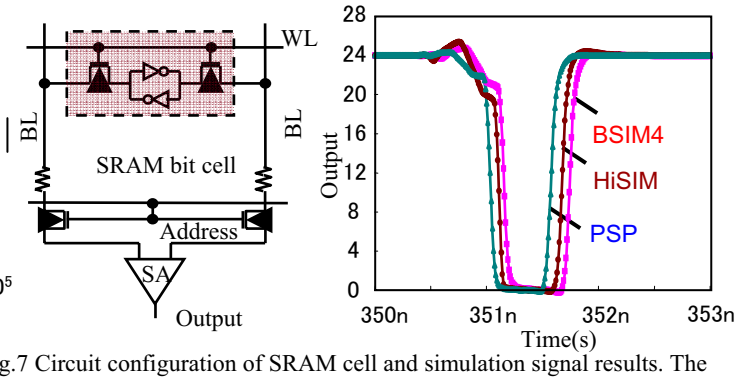

Fig.7 Circuit configuration of SRAM cell and simulation signal results. The number of nodes and elements are 11,973 and 24,145, respectively

Table II Simulation speed comparison results in 3 kinds of EDA vendor tools. Those are normalized by speed of BSIM4 model.

	A	B	C
BSIM4	1.00	1.00	1.00
PSP102	2.45	1.41	1.75
HiSIM2.3	1.59	1.07	1.42

Table III Summary of benchmark among BSIM4, PSP and HiSIM

	Param. extract	Conv.	Speed	IM3	1/f noise
BSIM4	+++	+++	+++	+	++
PSP102	+	+	+	++	-
HiSIM2.3.1	+++	+++	++	+++	++

- : Not evaluation