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Characterization and Modeling of Layout Dependent Parametric Variability of Nanometer Devices

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1. INTRODUCTION

Manufacturing variation of semiconductor devices has always been a major concern for both process engineers and designers as well. New techniques have thus been developed to increase the reproducibility of the manufacturing steps and to characterize and model the statistical component of the variation. These models are often expressed as worst case corner SPICE models that IC designers must use for the design optimization and verification before manufacturing. At the nanometer integration scale it is no longer possible to guarantee that all the layout patterns that the designers intend to print on silicon can be accurately reproduced for all possible corner combinations of the lithography equipment's tolerances. As a consequence the actual printed patterns may deviate significantly from the original design intent. Furthermore the complex interactions of layout 3D shapes with light determines the extent of such deviations which therefore are context dependent and vary substantially as a function of the neighborhood and local patterns. This layout/location dependent deviation from nominal or reference behavior may actually represent a significant fraction of the total variance. In this paper we will present an overview of the impact of parametric variation on device characteristics at nanometer nodes. We will discuss the break down of such variance into its main components (like e.g. die-to-die and within die, systematic and random) and we will finally present an empirical modeling methodology that can be used to quantify the effect of the systematic component.

2. Parametric Variability Characterization

Accurate and efficient characterization of the different types of variation places new requirements on the device characterization infrastructure. Statistically significant variability characterization requires large measurement samples, covering all major sources of variation. We have developed two types of test chips for variability characterization. The first is included as part of a full reticle test chip for characterizing the impact of front end of the line processing (FEOL) on yield and transistor performance and variability. This test chip contains test structures for statistically characterizing the impact of the main types of variation described in Section 1. The second test chip, called device scribe, contains a much smaller set of test structures suitable for monitoring transistor variation and its impact in mass production [1] .

These test structures are placed in the scribe line of product wafers. A novel addressable array test structure was developed to improve the packing and pad efficiency of the large number of test structures required for variability characterization. In addition, fast parallel parametric test hardware (pdFasTestII®) was developed and optimized to make use of the device arrays and minimize test time.

Together, the device array and fast parametric test hardware address the challenge of efficiently measuring the data required for statistically significant variability characterization. The test structure set contains four categories of structures for characterizing systematic variability from layout and neighborhood, across-chip variability characterization, leakage characterization, and support structures for decomposing the sources of variations. In addition to characterizing random variation, this set of structures covers most of the sources of layout driven variation discussed in literature, like proximity effects impacting lithography, stress effects, well proximity effects, poly step height effects. Test structures are designed to be sensitive to each of these effects, with the layout optimized to minimize the impact of other layout effects. A subset of the systematic variation patterns, especially those sensitive to patterning variation are selected for across-chip variability (ACV) evaluation. This is accomplished by placing them in device arrays and replicating these arrays multiple times across the reticle. Device arrays are particularly suited for across chip variability evaluation because they allow the measurement of many devices in a single test touchdown. A special configuration of device arrays, used in conjunction with fast parametric test, allows measurement of transistor characteristics on a large number of sites. By placing these structures on the scribe, potentially even die on every wafer can be measured in production [1]. This approach has been applied so far to measure up to 150 sites per wafer in production.

3. Components of parametric variation

Parametric variation can be categorized as either random or systematic. Random variation is the lot-to-lot, wafer-to-wafer, die-to-die and within die variation in identically designed transistors. Systematic variation is the change in transistor characteristics caused by the change in layout and local and global neighborhood of transistors with identically drawn gate length and gate width. As technology scales both the random and systematic components of variation increase.

For example,

Figure 1 shows the increase in NMOS Idrive variability from 90 nm to 65 nm technologies. The large variability of narrow width devices, which are used in SRAM bit cells and low-power designs makes problem of variability especially urgent for the designs employing narrow width transistors.

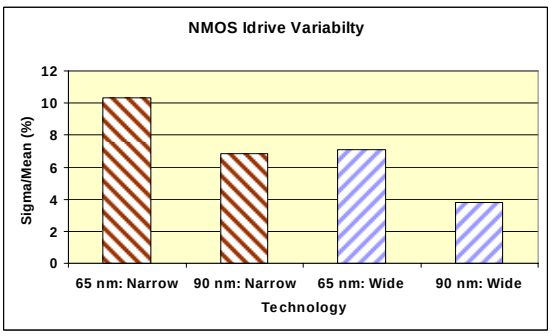

Figure 1: NMOS Idrive variation over multiple generations

As we stated before, transistors behave differently based upon the neighborhood layout pattern due to printability, OPC capability stress and other 3D effects. Figure 2 shows the Idrive vs. Ioff currents for identical transistors in three different layout environments in 65nm technology. As depicted in the figure, depending on effectiveness of the OPC, there can be as much as 40% difference in the mean values of Idrive and two orders of magnitude difference in the mean values of Ioff between these transistors placed in gate poly environments I and III, respectively.

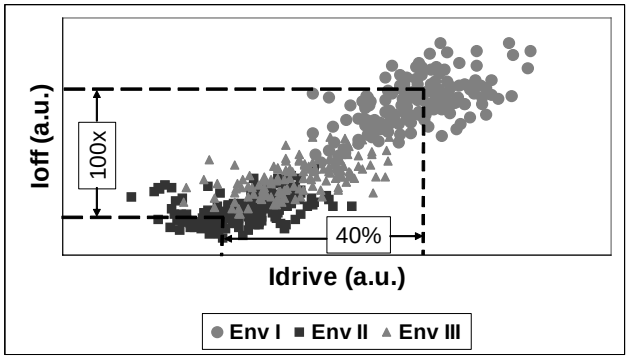

Figure 2: Impact of gate neighborhood on transistor performance

4. Layout dependent macro-models

As shown in the previous section, a significant fraction of the total transistor parameters variance is actually related to geometrical and neighborhood dependent effects. It is therefore critical to model such deterministic behavior in order to reduce the total (unexplained) device variance which shall then be taken into account by statistical and corner models.

A number of modeling techniques have been proposed to address this issue (as for example in [2], [3]) . Most of these techniques attempt to model layout attribute dependent effects in terms of physical root causes such as device length variation or reticle stress. Physically based modeling is however quite difficult, as it is not easy to separate and model complex effect's interactions, such as for example W and L variation impact on device capacitance.

We have developed an empirical macro-modeling methodology which addresses this problem by describing incremental device characteristics as a function of ideal transistor parameters and layout attributes.

For example let's assume that a set of device characteristics such as saturation currents and threshold voltages are measured for a set of devices whose layout attribute parameters are made to vary according to a particular Design Of Experiments (*D.O.E.*). Let the vector X= $x_1,\ldots,x_n$ represent the values of the input parameters of such a DOE. Let define the device corresponding to the central point of such a DOE as the *reference* device and let i_{ds}^{ref} represent its saturation current. We attempt to model the *incremental* current component due to non-ideal behavior caused by layout and neighbor effects as:

(1) $\Delta i_{ds} = f(i_{ds}^{ref}, W, L, x_1,\ldots,x_n)$

where W/L are the width and length of the reference device. The actual functional representation of the incremental current Δi_{ds} in equation (1) can be modeled by its Response Surface:

(2) $\Delta i_{ds} = c + BX + X^T AX$

and the value of the unknown coefficient matrices *A, B, c* can be estimated by maximizing the fraction of variance of the experiment matrix that is explained by the response surface model (2).

5. Application example

The empirical characterization of the systematic layout dependent effects described in the previous section has been applied to several different process technologies at the 90, 65 and 45nm nodes. An example of the typical results is shown in Figure 3.

The data (hollow markers with error bounds) represent the median of a set of measurements of 8 NMOS devices with identical W/L but different layout configurations (i.e. 3 different contact placement styles and 3 different drain extensions). The lines represent the predictions of our systematic macro-models, which are shown to be in excellent agreement with the experimental results.

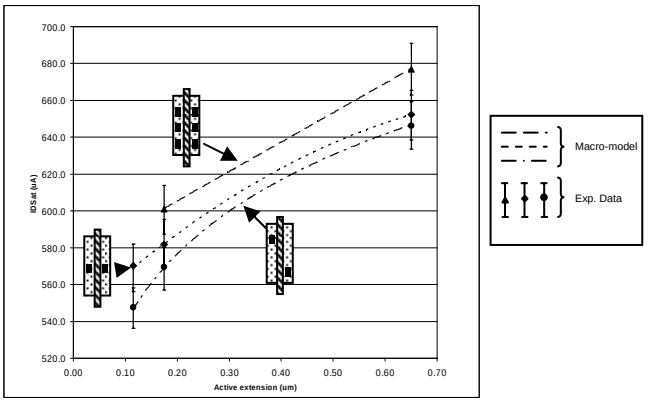

Figure 4: Empirical macro-modeling results

6. Conclusions

In this paper we have presented an overview of the impact of parametric variation on MOSFET devices in nanometer technologies. We have shown that a significant fraction of the total device variability is caused by systematic, layout dependent effects, and we have presented an empirical macro-modeling methodology that allow to accurately explain the systematic portion of the total variance that is observed in a set of measurement data, thus allowing to significantly narrow down the portion of variability that needs to be taken into account during circuit design optimization and verification.

7. References

[1] M. Quarantelli et al, "Characterization and Modeling of MOSFET Mismatch of a Deep Submicron Technology", IEEE Int. Conference on Microelectronic Test Structures, 2003

[2] C. Munkang, L. Milor, L. Capodieci, "Simulation of the circuit performance impact of lithography in nanoscale semiconductor manufacturing", SISPAD 2003

[3] A. Shibkov, V. Axelrad, , "Integrated Simulation Flow for Self-Consistent Manufacturability and Circuit Performance Evaluation", SISPAD 2005