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Investigation of Matching Performance for Uniaxial Strained PMOSFETs

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Introduction

To enable the mobility scaling, strained silicon is widely used in state-of-the-art CMOS technologies [1-2]. While the carrier mobility enhancement can help overcome the speed/power barrier for logic applications, the impact of strain on analog performance is another important issue that has to be considered for strained MOSFETs. Although several studies have investigated the analog performance of strained devices recently [3-4], the impact of strain on matching properties has rarely been examined. Through a comparison between strained and unstrained devices, this work investigates the matching performance of uniaxial strained PMOSFETs [2] with sub-100 nm gate length.

Experimental

Co-processed strained and unstrained PMOSFETs are investigated in this study. The strained devices were fabricated by state-of-the-art process-induced uniaxial strained-silicon technology featuring SiGe source/drain and compressive Contact Etch Stop Layer (CESL) [4]. For the transistors with gate length L_{gate} =54 nm, the saturation drain current (I_{dsat}) of the strained device is improved more than 100% as compared with its control counterpart.

The matching properties of the strained and unstrained devices are extracted from identical devices in a matching pair configuration on 50 dies. Statistics on the mismatch in drain current ($(\Delta I_d)/I_d$) and threshold voltage (ΔV_{th}) in the linear region were obtained. Since analog circuits are usually biased in the low gate-bias (V_g) regime (e.g., $V_{gst}=V_g - V_{th}$=0.2V) for better power efficiency [5], this study will focus on the matching properties in the low V_{gst} regime.

Results & Discussion

Fig. 1 shows the V_g dependence of the extracted standard deviations of drain current mismatch ($\sigma(\Delta I_d)/I_d$) for strained and control devices with L_{gate} = 54nm and gate-width (W) = 1μm and 0.3μm. It can be seen that the $\sigma(\Delta I_d)/I_d$ of the strained device is larger than that of the unstrained one in the low V_{gst} regime. In other words, the matching performance is degraded in the low V_{gst} regime for the strained device.

The drain current mismatch in the low V_{gst} regime is dominated by the threshold voltage mismatch [6], and can be expressed as [7]:

$$\frac{\Delta I_d}{I_d} = -\frac{g_m}{I_d} \times (\Delta V_{th}) \qquad (1)$$

where g_m is the transconductance. To verify the relevance of ΔV_{th} to $\Delta I_d/I_d$, Eq. (1) can be rewritten as $(\Delta I_d)/g_m = -\Delta V_{th}$ [8] and the correlation (ρ) between $(\Delta I_d)/g_m$ at V_{gst} = 0 and $(\Delta I_d)/g_m$ at other V_{gst} is shown in Fig. 2. It can be seen from Fig. 2 that the correlation lies between 70% and 100% for both strained and control devices. This ensures that the threshold voltage mismatch is the dominant mechanism that determines the drain current mismatch in the low V_{gst} regime.

Fig. 3 shows the Pelgrom plot [9] of ΔV_{th}. The geometry of the strained device in Fig. 3 are W/L_{gate}=1μm/54nm and 0.3μm/54nm. Note that the L_{gate} of the strained device needs to be the same in order to keep similar strain in the channel. This is because the channel strain is gate-length dependent in process-induced strain silicon devices [10]. From Fig. 3, it can be seen that the area dependence of $\sigma(\Delta V_{th})$, A_{Vth}, are almost the same for the control and strained device. This is consistent with the area dependence of $\sigma(\Delta I_d)/I_d$, A_{Id}, as shown in Fig. 4. However, the discrepancy in $\sigma(\Delta I_d)/I_d$ between the control and strained devices (Fig. 4) is significantly larger than the discrepancy in $\sigma(\Delta V_{th})$ (Fig. 3) when one-to-one device comparison is made. This can be explained by the g_m/I_d plot shown in Fig. 5.

In the linear region, g_m/I_d can be modeled by [11]:

$$\frac{g_m}{I_d} = \frac{1}{V_{gst} - V_d/2} + \frac{d\mu_{eff}/dV_g}{\mu_{eff}} \qquad (2)$$

where μ_{eff} is the carrier mobility. The larger g_m/I_d for the strained device (Fig. 5) than its control counterpart at a given V_{gst} can be attributed to the gate-bias sensitivity of the carrier mobility, the second term in Eq. (2).

Fig. 6 shows the extracted carrier mobility [4] versus V_{gst}. It can be seen that μ_{eff} increases with V_g in the low V_{gst} regime (e.g., V_{gst} = 0.2 V). This is because in the low V_{gst} regime, the mobility is mainly determined by Coulombic scattering. The mobile carrier screening makes μ_{eff} increases with V_g. The larger slope of the mobility for the strained device[4] is responsible for the higher g_m/I_d observed in Fig. 5.

Fig. 7 shows $\sigma(\Delta I_d)/I_d$ versus normalized drain current for strained and control devices. For analog devices biased by constant drain current, Fig. 7 indicates that the strained device has worse matching performance than its control counterpart. Fig. 8 and Fig. 9 show the correlation ρ and g_m/I_d versus normalized drain current, respectively. The larger drain current mismatch for devices biased by constant drain current than by constant V_{gst} can be attributed to the larger g_m/I_d enhancement of the strained device under constant drain current.

Conclusions

We have investigated the matching properties of uniaxial strained PMOSFETs with sub-100 nm gate length. In the low V_{gst} regime, the area dependences of the drain current mismatch and the threshold voltage mismatch are similar for control and strained devices. When one-to-one device comparison is made, nevertheless, the drain current mismatch for the strained device is degraded because of the enhanced g_m/I_d. The enhanced g_m/I_d can be attributed to the higher V_g sensitivity of the carrier mobility present in the strained device. For analog devices biased by constant drain current, the strained device also shows worse matching properties. Although g_m/I_d is superior for the strained device, the resulting worse matching performance needs to be considered when using these advanced strained devices in analog design.

Acknowledgement

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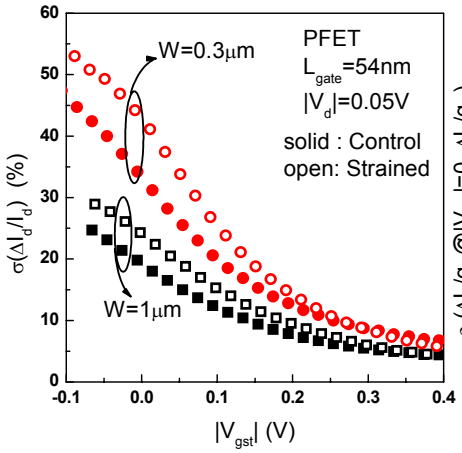

Fig. 1 $\sigma(\Delta I_d)/I_d$ vs. V_{gst} shows larger drain current mismatch for the strained device.

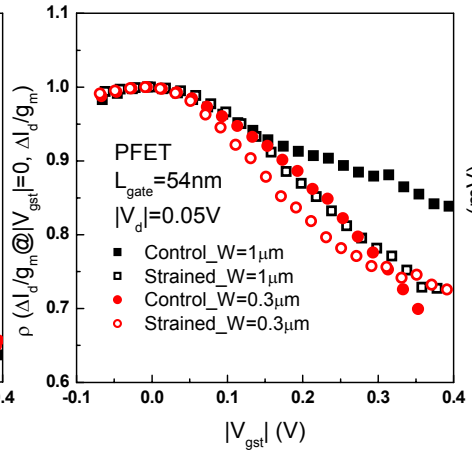

Fig. 2 Correlation (ρ) between $(\Delta I_d)/g_m$ at V_{gst}=0 and $(\Delta I_d)/g_m$ at other V_{gst} vs. $|V_{gst}|$. The high correlation coefficient ensures the relevance of the threshold voltage mismatch (ΔV_t) to the drain current mismatch ($\Delta I_d/I_d$).

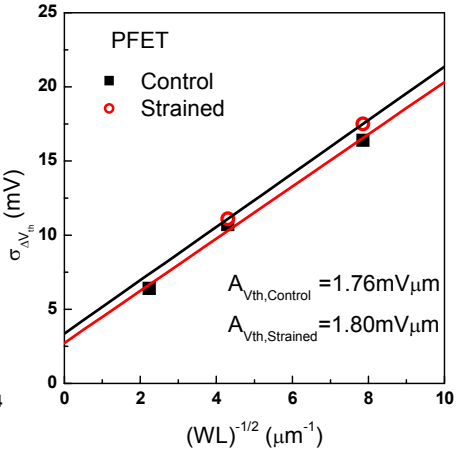

Fig. 3 $\sigma(\Delta V_t)$ vs. $(WL_{gate})^{-0.5}$ shows similar area dependence of $\sigma(\Delta V_t)$ for the strained and control device.

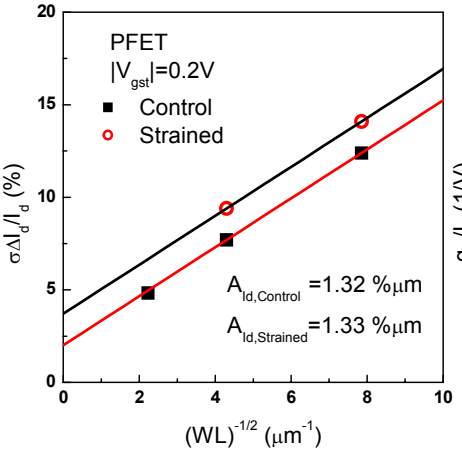

Fig. 4 $\sigma(\Delta I_d)/I_d$ vs. $(WL_{gate})^{-0.5}$ shows similar area dependence of $\sigma(\Delta I_d)/I_d$ for the strained and control device.

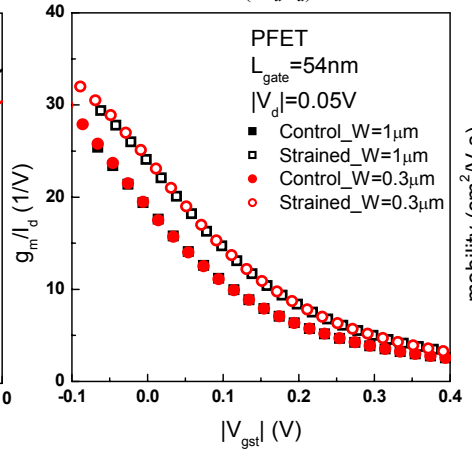

Fig. 5 g_m/I_d vs. $|V_{gst}|$ showing the strain-enhanced g_m/I_d in the low V_{gst} region.

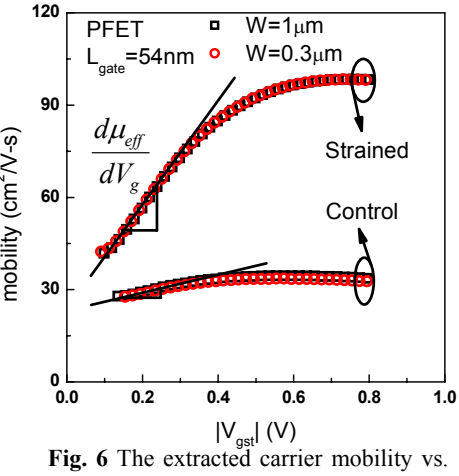

Fig. 6 The extracted carrier mobility vs. $|V_{gst}|$ shows larger V_g sensitivity of carrier mobility in the low V_{gst} region for the strained device.

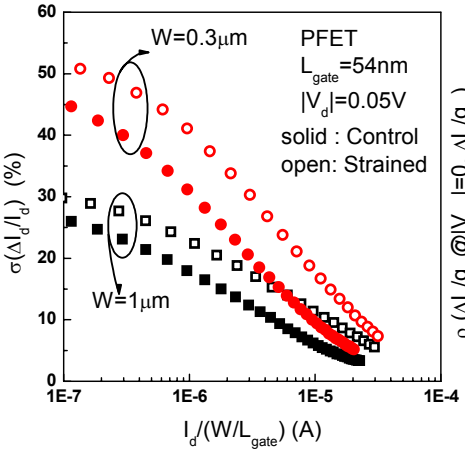

Fig. 7 $\sigma(\Delta I_d)/I_d$ vs. normalized I_d shows larger drain current mismatch for the strained device.

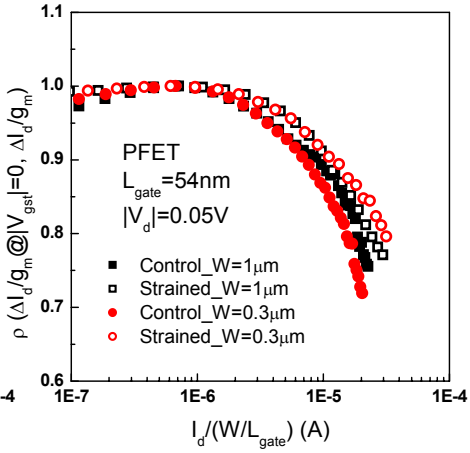

Fig. 8 Correlation (ρ) between $(\Delta I_d)/g_m$ at V_{gst} = 0 and $(\Delta I_d)/g_m$ at other V_{gst} vs. normalized I_d.

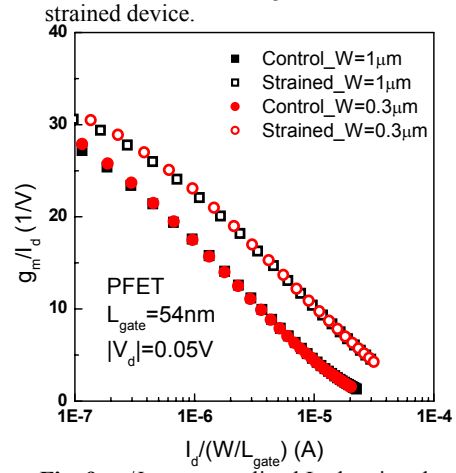

Fig. 9 g_m/I_d vs. normalized I_d showing the strain-enhanced g_m/I_d.