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Novel Soft Error Hardened Latches and Flip-Flops

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1. Introduction

Soft errors are transient errors induced by radiation. The main causes in terrestrial environments are neutrons as secondary cosmic rays and alpha particles from LSI materials. We have proposed a simulation system for calculating soft error rates (SER) in LSI chips [1, 2]. Figure 1 shows the SER of each technology generation of chip. In SRAMs, an error correction code (ECC) dramatically reduces soft errors. However it is difficult to apply ECC to FF circuits, so it is very important to develop techniques for mitigating soft errors in latches and FFs. T. Calin et al. proposed a tolerant latch as shown figure 2 that achieved a 10 times lower SER at 1.0V [3][4]. However, these latches will not avoid all soft error problems.

In this paper, we propose new soft error robust latches and FFs. We have estimated these robust efficiencies for soft errors and have demonstrated their superiority. In addition, we have designed a modified robust FF including the proposed latch and have calculated its overheads from the conventional robust latch [3].

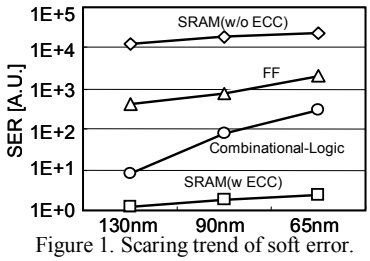

Figure 1. Scaring trend of soft error.

Table 1 Simulated chip detail.

	130nm	90nm	65nm
SRAM	2Mb	4Mb	8Mb
FF	100kb	200kb	400kb
Freq.	500MHz	1GHz	2GHz

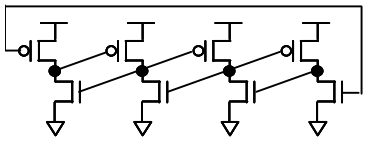

Figure 2. Conventional robust latch [3].

2. Soft Error Hardened Latch Circuit

We propose new latch circuits which are robust against soft errors. This proposed latch circuit consists of four gates as shown in Figure 3 (a). The latch has four data nodes. Each gate has two-inputs and one-output as shown in Figure 3 (b). Even if the data of one node becomes corrupted, the gate does not propagate the corrupted data to the other nodes. This is because one node of the latches receives feedback from two other nodes that keep the correct data. As a result, these latches efficiently reduce soft errors. Many variations like Figure 4 can be constructed as the robust latches.

We investigate the characteristics of these latches by applying various noise current to each node of the robust latches (Fig. 4). These latches are designed with 65-nm technology node, bulk CMOS-FET and 9-grid height and an operating voltage of 1.0V. Table 2 summarizes the number of transistors of each latch and the simulated results. The "Q0" is collected charge and the noise currents applied by using the double exponential model by HSPICE [5].

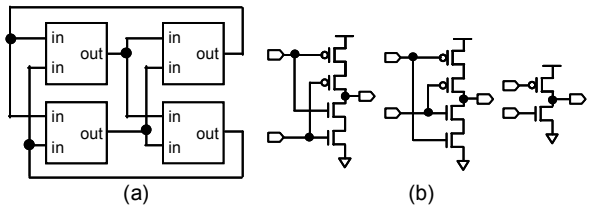

Figure 3. (a) Structure of robust latch and (b) two-input gates.

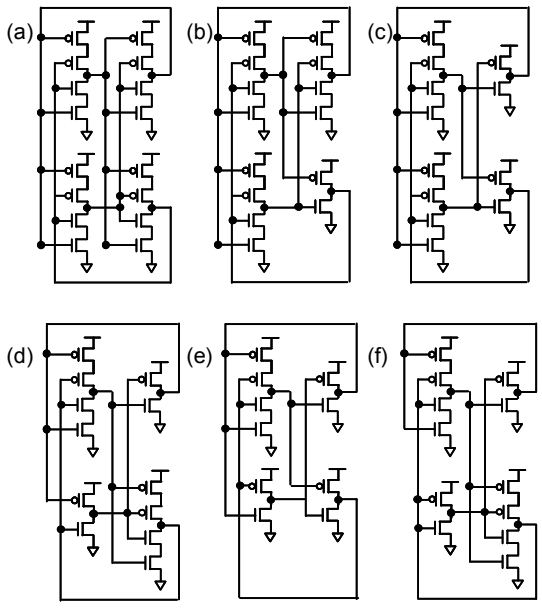

Figure 4. Proposed robust latches.

Table 2. Soft error immunity against various noise currents.

	Tram. Num.	Q0= 10fC	Q0= 20fC	Q0= 50fC	Q0= 100fC
(a)	16	No Error	No Error	No Error	No Error
(b)	14	No Error	No Error	No Error	No Error
(c)	12	No Error	No Error	No Error	**Error**
(d)	12	No Error	No Error	No Error	**Error**
(e)	10	No Error	No Error	No Error	**Error**
(f)	12	No Error	No Error	**Error**	**Error**

The new robust latches show excellent tolerance but errors are occurred by the noise of which the Q0 is 100fF in some latches. We focus on the latch shown in Figure 4 (e) because of its efficiency (the number of transistors and immunity against soft errors) and discuss upset phenomena in latches more accurately.

We design the latch as shown in Figure 5 (a) and calculate the characteristics. We calculate the node current by a device simulator for accurate simulation. We investigate the current when a particle having linear energy transfer (LET) of 0.2pC/um is incident on the drain diffusion region of an nMOS transistor. The current is calculated using the device simulator DESSIS. Figure 5 (b) shows the detailed setup of the device simulation.

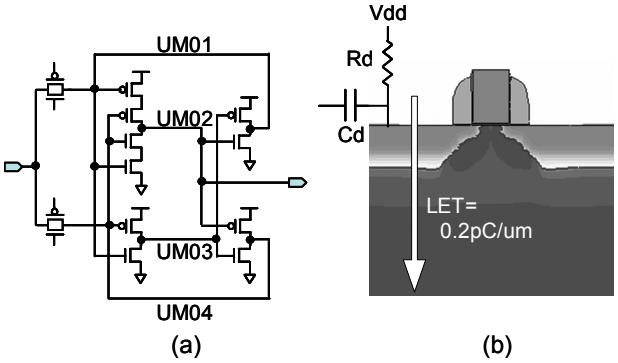

Figure 5. Simulated (a) circuit and (b) device detail.

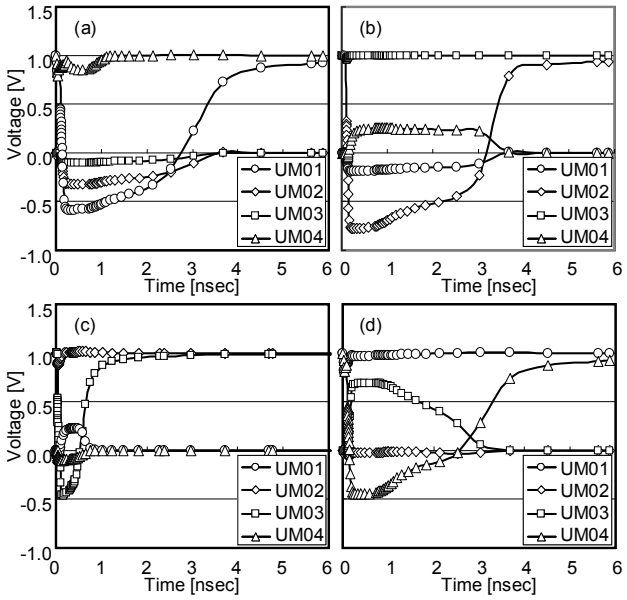

Figure 6. Voltage waveforms in robust latch as shown in figure 5 (a) occurring a noise at (a) UM01, (b) UM02, (c) UM03 and (d) UM04.

The current waveforms are calculated with the Rd and Cd derived from the circuits. The voltage variations by a particle penetration of the new robust one are calculated with the calculated current waveform. Figures 6 show the voltage variations on each node in proposed robust latches respectively.

In the proposed new latches, each node is not corrupted even if noise occurs on any node. This precise simulation proves that in the proposed new latches, corruption does not occur soft errors under various noises and that the latch has excellent tolerances against soft errors. When a neutron in a terrestrial environment collides with Si, the generated particles with the LET greater than 0.2pC/um is negligible [2]. The LET of alpha particles is lower than that of the particle generated by the neutron. The collected charges (Q0) are more than 120fC on every node in the robust latch according to results by the device simulation with the LET of 0.2pC/um.

This means that soft errors will not occur in the proposed robust latch in terrestrial environments. The robust latch shown in Figure 4 (e) is perfect hardened one with increasing by only two transistors compared with the conventional robust latch in terrestrial environment.

3. Soft Error Hardened Flip-Flop Circuit

We design a master-slave Flip-Flop circuit using conventional robust latches [3] and that using the proposed robust latches for estimating overheads. These Flip-Flops has the function of scan and clock asynchronous reset and is also designed with 9-grid height and 65-nm technology. The main characteristics of these two FFs are summarized in Table 3. The overheads of the new robust FF are a little than the FF used conventional robust latch.

Table3 Characteristics in conventional robust Flip-Flop and new robust Flip-Flop

	Conventional Robust	New Robust
Size	1	1.02
Delay	1	1.00
Setup	1	1.00
Power(Data)	1	1.03
Power(Clock)	1	1.00

4. Conclusion

In this study, we proposed robust latches against soft errors. By conducting precise analyses, we showed that soft errors are prevented in the proposed new latches in terrestrial environments. In addition, we designed a FF circuit using conventional robust latches and using the new robust latches. The overheads of the new robust FF are a little than the FF used conventional robust latch. These results indicate the excellent performance of the proposed FF reducing soft errors with a little overheads.

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