

Evaluation of Digital Crosstalk Noise on a Differential Input VCO

Akihiro Toya¹, Yoshitaka Murasaka², Takafumi Ohmoto² and Atsushi Iwata^{1,2}

¹Hiroshima University, 1-3-1 Kagamiyama, Higashi-hiroshima, Hiroshima, 739-8530 Japan

Phone: +81-824-24-7641 E-mail: akihiro@dsl.hiroshima-u.co.jp

²A-R-Tec Corp., Campus Bldg 209, 5-10-7 Saijoshitami, Higashi-hiroshima, Hiroshima, 739-0047 Japan

1. Introduction

With the progress of device scaling in CMOS mixed signal LSIs, digital crosstalk noise transferred to the analog circuits through silicon substrate becomes a serious problem. The noise reduces the signal-to-noise ratio of amplifiers and increases the jitter of clock generators.

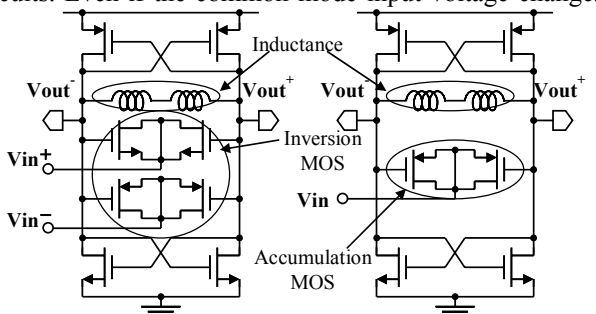
The purpose of this study is to measure and evaluate the effect of digital crosstalk noise on a differential input Voltage-Controlled Oscillator (VCO) comparing with a conventional single input one.

2. VCO

The VCO generating a periodic signal is widely used as clock generation circuits for digital circuits and local oscillators of RF transceiver. The output frequency of VCO is controlled by an input voltage and its performance is evaluated by output phase noise and jitter.

Performance Index: We evaluate phase noise of VCO as a performance index in the frequency domain and cycle-to-cycle jitter and cycle-jitter as performance indices in the time domain. The cycle-jitter is estimated from the period (T_i) of oscillation waveform and the cycle-to-cycle jitter is estimated from the difference in periods from one cycle to the next ($T_i - T_{i-1}$). The cycle jitter is caused by low frequency component of noise and cycle-to-cycle jitter is caused by high frequency component. Each type of jitter was evaluated by the standard deviation (σ) and peak-to-peak (p-p) value.

Circuit configuration of VCO: A differential-input LC VCO using complementary variable capacitors composed of p- and n- inversion-MOSs, is shown in Fig. 1 along with a single-input LC VCO using an accumulation-MOS variable capacitor. The structures of the inversion and the accumulation devices are shown in Fig. 2. The differential control voltages with DC level around the threshold voltages of n- and p-MOS are supplied through level shifting circuits. Even if the common mode input voltage changes,



(a) Differential-input VCO (b) Single-input VCO
Fig. 1 Single and Differential-input VCOs

the total capacitance of the varactor is constant. Therefore, the differential-input VCO is insensitive to the change in common-mode of the control voltage.

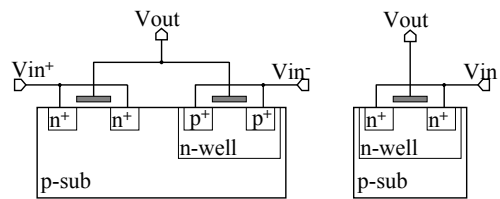
3. Test Chip Design

To measure and evaluate the influence of substrate noise, a user-controllable noise generator and a set of noise detectors are necessary. Selected for this study were transition controllable noise source (TCNS) and noise waveform detector (NDET), both of which were proven useful for substrate noise evaluation.[1,2] The TCNS has a nine-stage variable delay circuit which drives an array of 32 blocks of CMOS inverter arrays. The delay time and the number of blocks being activated (0-32) are controllable. When the delay is set to the minimum 0.48nsec, the noise voltages injected from the nine arrays are superimposed. The resulting noise waveform in the substrate has one large peak at the transition time followed by ringing. While the TCNS is operated periodically, the NDET measures the periodic noise waveform using the equivalent sampling technique. The input of each detector is connected to a probing point on the substrate contact or a GND wire. The voltage resolution and timing resolution of NDET are 100uV and 100ps, respectively.

The test chip, shown in Fig. 3, was fabricated in a 0.25um CMOS technology. To measure the influence of the substrate noise, the proposed differential-input VCO (VCO1), the conventional single-input VCO (VCO2) for comparison, two TCNSs, and NDETs are integrated on the chip. The probes of NDETs sense the potential changes of substrate near VCO and the GND line. The measured noise waveforms when the total number of TCNS's active blocks is 64 are shown in Fig. 4.

4. Measurement results

Frequency vs. control voltage: Measured f-V characteristics of VCO1 are shown in Fig. 5. VCO1 has a gain of 147MHz/V for a differential-mode input voltage, and 700kHz/V for a common-mode input voltage. The VCO1 is robust to common-mode changes in the control voltage.



(a) Inversion MOS (b) Accumulation MOS
Fig. 2 Structures of MOS varactors

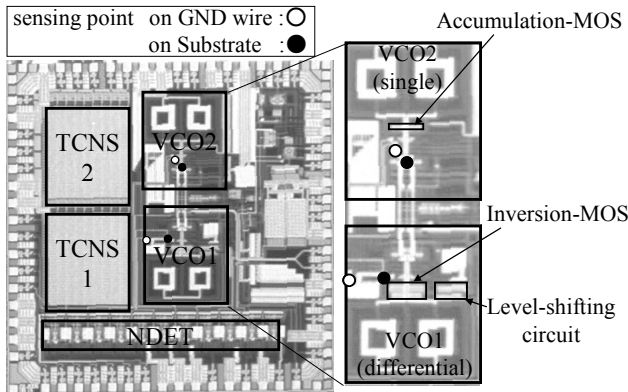
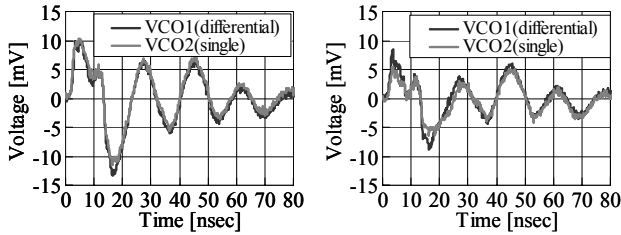
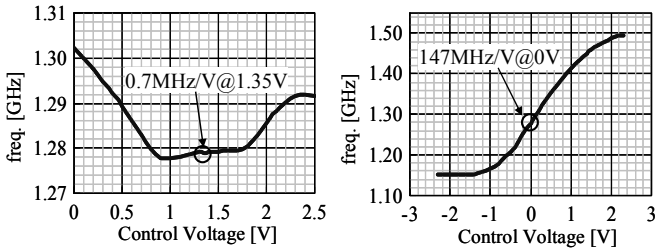


Fig. 3 Test chip photograph



(a) Substrate noise (b) GND wire noise

Fig. 4 Substrate and GND wire noises



(a) Vs common-mode input (b) Vs differential-mode input
Fig. 5 Measured f-V characteristics of VCO1

Phase noise and jitter: The phase noise characteristics are shown in Fig. 6. While VCO1 has the same gain as VCO2, the phase noise of VCO1 at 100kHz offset frequency is 10dB smaller than VCO2. When VCO1 is compared with VCO2, the standard deviation of cycle-to-cycle jitter was improved from 5.07psec to 4.21psec, but that of cycle jitter was degraded from 2.59psec to 3.00psec.

Effect of cross talk noise: The output jitter of each VCO was measured as a function of the TCNS noise blocks (16, 32, and 64) to evaluate the influence of substrate noise. The TCNS clock frequency was 27MHz. The measured cycle jitter and cycle-to-cycle jitter are shown in Fig. 7. Under any of the conditions of noise magnitude, measured cycle jitter of VCO1 is at least 10% smaller than that of VCO2, but the cycle-to-cycle jitter is about 30% larger. It indicates that VCO1 is affected by low frequency noise. The reason is as follows. The back-gate of n- inversion MOS directly connects to the substrate. On the other hand, p-MOS varactor is formed in the n-well which is connected to the substrate through a junction capacitance. Thus noise cancellation effect of VCO1 is reduced for low frequency components. For high frequency noise, VCO1 is relatively insensitive and its jitter is lower than that for low frequency noise. Noise cancellation characteristics for low frequency

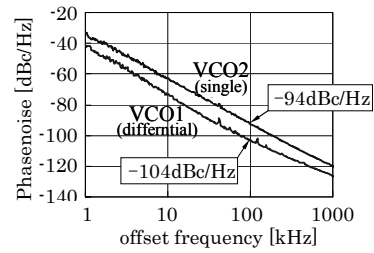
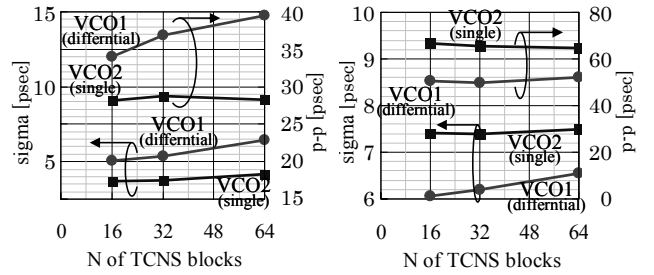


Fig. 6 Measured phase noise of VCO1 and VCO2



(a) Cycle jitter (b) Cycle-to-cycle jitter

Fig. 7 Measured jitter vs. N of active TCNS blocks

components can be improved by using a triple well structure.

5. Conclusion

A differential-input VCO with inversion-MOS as a varactor was designed and fabricated along with a conventional single-input VCO for performance comparison. From the measurement results, we confirmed that phase noise was improved by 10dB at 100kHz offset frequency, compared with the conventional single-input VCO. The effect of the substrate cross talk noise to the VCO jitter was also measured with the on-chip noise source and detectors. The cycle-to-cycle jitter of the differential-input VCO was 10% smaller than that of the single-input VCO in the presence of substrate noise generated by the 64 TCNS blocks and 27MHz of the TCNS clock frequency.

Acknowledgements

I would like to thank parties concerned in the project. This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc., Synopsys Corporation and Mentor Graphics Corporation.

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