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LSI on-chip optical interconnection with Si nano-photonics

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1. Introduction

As the scaling of CMOS technology proceeds, it will become increasingly difficult for conventional copper interconnect to satisfy the design requirements of delay, power, bandwidth, and noise. On-chip optical interconnects have been considered as a potential substitute for electrical interconnects [1, 2].

Recent progress in optical technology is now making such LSI on-chip interconnections more realistic [3]. Si nano-photonics is a key technology for realizing such optical components on an LSI chip, where essential optical components can be fabricated with Si CMOS-compatible device processes [4].

In this paper, we report the advantage of optical interconnects at different LSI technology nodes based on a practical prediction of optical device development. We also report on basic optical components used to build an on-chip optical interconnection. Advanced circuit designs for high-speed clock distribution with waveguide-integrated Si nano-photodiodes (PDs) are also discussed.

2. Structure of LSI on-chip interconnection

A. Comparison between optical and electrical interconnects

Figure 1 shows a schematic cross-sectional image of a prototype optical chip integrated structure on an LSI chip that we have proposed [5]. An optical chip is electrically connected with an LSI chip using solder bumps and Cu vertical via wiring formed on an optical layer.

On-chip optical interconnections can be used in several ways for sending/receiving data signals within an LSI chip. For example, optical clock distribution and on-chip optical bus connection are representative applications [6].

Figure 2 shows the power-delay product (PDP) dependence on interconnect length in electrical and optical wiring for each technology node. Optical interconnects have an overhead in PDP, which arises from OE/EO conversion. Especially, lowering of power in EO conversion with a Si-based EO modulator is a particular challenge for Si photonics, and great efforts have been made for higher performance and a smaller footprint [7]. Our proposal is a nano-crystalline EO material of PLZT (lanthanum-doped lead zirconium titanium oxide)-based modulator, which has a much larger EO coefficient [8], and a potential of lower operation voltage with a ring resonator structure [9].

Based on a practical prediction of our optical device development, we can reduce the consumption power of OE/EO devices and that of their driver circuits along with the scaling of the LSI technology. At hp32-22 nm, optical interconnect will then have an advantage over electrical interconnects within a chip that has an interconnect length less than about 10 mm. Global optical interconnects are also expected to realize seamless signal transmission with an inter-chip optical communication system and give a good solution for LSI pin bottleneck problem by introducing wavelength division multiplexing (WDM) architecture.

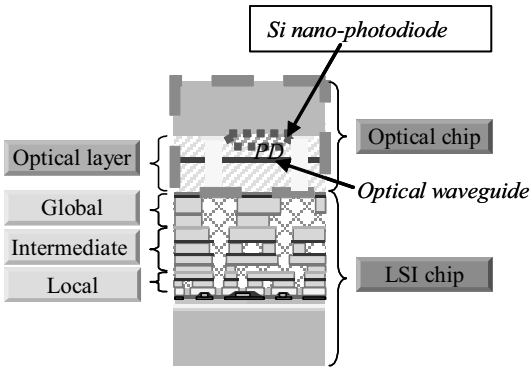

Fig. 1 Schematic cross-sectional image of optical chip integrated on LSI chip [5].

B. Development of on-chip optical clock distribution

We developed a component for optical clock distribution to demonstrate the advantage of the on-chip optical interconnect from the viewpoints of jitter, skew, and delay. In the prototype structure, optical clock distribution utilizes four PDs connected to optical waveguide branches. Fundamental clock signals are delivered from a 10-20 GHz

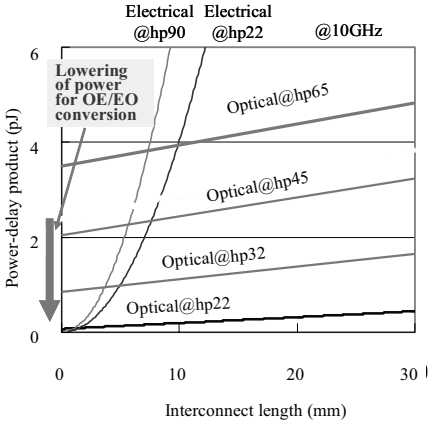

Fig. 2 Power-delay product dependence on interconnect length in electrical and optical wiring for each technology node [5].

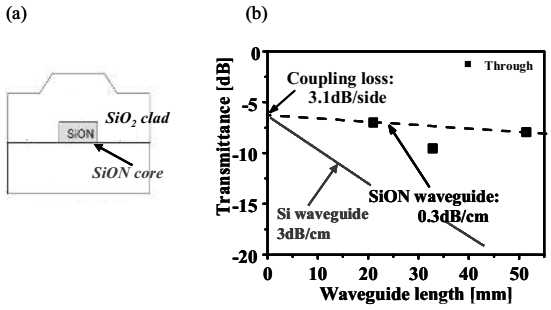

Fig. 3 (a) Schematic cross-sectional image [5, 10], and (b) insertion loss vs. waveguide length [5, 11].

mode-locked laser system with a 780 nm wavelength, which is located outside the LSI chip.

Figure 3 shows a schematic cross-sectional image of a SiON (silicon oxynitride) waveguide [5, 10], and its insertion loss characteristics are shown compared with those of a Si channel waveguide [5, 11]. The propagation loss of the SiON waveguide was estimated to be 0.3 dB/cm, which is about one order smaller than that of the Si waveguide. A high-accuracy 3-dB branch of a multi-mode interference structure was also developed for optical clock distribution [10].

For clock distribution with an H-tree structure, a small footprint of a photodiode should be efficiently connected to the optical waveguides. Figure 4 shows required light source power dependence on PD capacitance to clock the LSI circuit at 10 GHz, which was calculated using a model in which the CMOS input capacitance and PD capacitance are electrically charged by a generated photocurrent [4]. With a decrease in PD capacitance, the required light source power decreases and saturates at the CMOS input capacitance charging energy, which is one order of magnitude smaller than that of a conventional PD system. To achieve extremely low power consumption, PD capacitance should be decreased to less than several fF.

The Si-based PD is the most desirable for on-chip fabrication. However, a fast response Si PD usually results in poor efficiency, because of the relatively small absorption coefficient of Si. To overcome this problem, a surface plasmon antenna that realizes optical energy confinement within a subwavelength region and enhances efficiency for a Si nano-PD has been developed [12, 13]. We developed a

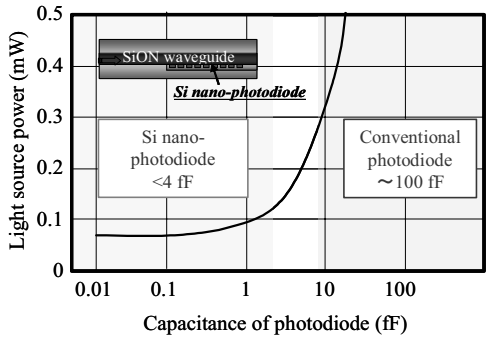

Fig. 4 Light source power dependence on capacitance of photodiode for 10 GHz optical clock circuit [4].

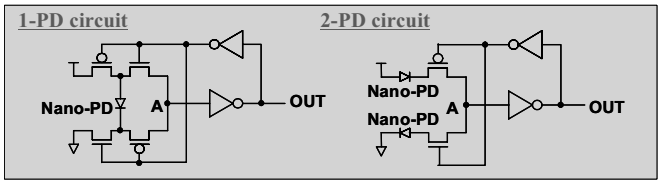

Fig. 5 Schematic diagram of optical clock circuit [4].

SiON waveguide integrated Si nano-PD that has nano-scale Ag electrode arrays at the interface between the SiON core and the Si absorption layer. Si nano-PDs were designed to have enhanced speed and efficiency with a small capacitance of less than 4 fF [14].

Figure 5 shows a schematic diagram of an optical clock circuit that we have proposed [4]. In a conventional optical signal detection system, transimpedance-amplifiers (TIAs) are necessary to match the impedances between the PD and electrical circuits. For on-chip interconnections, we have proposed an advanced TIA-less clock circuit in which CMOS circuits are driven by a push-pull operation with a direct electrical charge from a Si nano-PD, resulting in less power consumption and clock signal distribution with a small jitter/skew/delay at more than 10 GHz [4].

3. Conclusion

LSI on-chip optical interconnections were discussed from the viewpoint of a comparison between optical and electrical interconnections. Fundamental optical devices and components used in interconnections were also introduced that are small enough to be placed on top of a Si LSI and with CMOS process compatible fabrication methods. Above 10-GHz clock distribution can be achieved by using TIA-less optical clock distribution circuits with a small footprint.

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References

[1] D. A. B. Miller, Proceedings of the IEEE **88**, (2000) 728.
[2] D. A. B. Miller et al., ISSCC Dig. Tech. Papers (2005) 86.
[3] M. J. Kobinsky et al., Intel Technology Jounal **8**, (2004) 129
[4] K. Ohashi et al., ISSCC Dig. Tech. Papers (2006) 426.
[5] K. Ohashi, MIRAI-Pj III 2006 Annual Report.
[6] K. Nishi et al., Extended Abstract of the 2006 SSDM (2006) D-5-1.
[7] Q. Xu et al., Nature **435**, (2005) 325.
[8] M. Nakada et al., Jpn. J. Appl. Phys. **44**, (2005) L1088.
[9] T. Shimizu et al., IEEE/LEOS GFP 2007, to be published.
[10] T. Watanabe et al., Proc. 2007 IEICE Gen. Conf., (2007) 232.
[11] A. Gomyo, et al., Extended Abstracts (The 68th Autumn Meeting, 2007); Jpn. Soc. Appl. Phys., to be published.
[12] T. Ishi et al., Jpn. J. Appl. Phys. **44**, (2005) 364.
[13] J. Fujikata et al., Extende Abstract of the 2005 SSDM (2005) E-3-3.
[14] J. Fujikata et al., Extended Abstracts (The 68th Autumn Meeting, 2007); Jpn. Soc. Appl. Phys., to be published.