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Passive Optical Alignment with High Accuracy for Low-Loss Optical Interposer

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1. Introduction

The performance of large-scale integration (LSI) has been improved by scaling down the device size. However, the I/O circuits in LSI need much power to drive the external wiring with large capacitances and inductances in package and print circuit boards (PCBs). In addition, the capacitance and inductances have many problems such as electromagnetic interference (EMI), cross-talk noise, and jitter. As the increase in the data transmitting speed, these problems become more serious for electrical circuits. Therefore, the circuits are complicated to provide high signal performance. To overcome these problems, optical interconnections instead of the electrical ones have been of great interest for the high speed data transfer [1]-[3] although several technical challenges are presented in the optical interconnections. One of the biggest problems is the precise alignment between optical waveguides and vartical-cavity serface-emitting laser diodes (VCSELs)/ photo diodes (PDs). Passive optical alignment has a big advantage of the tact time over the active optical alignment with optical instruments such as a laser, a PD, and a precise fiber-positioning station. Another problem is the difficulty in integrating VCSELs/ PDs on an LSI chip or an interposer because VCSEL that is a representative GaAs compound device is hardly fabricated with Si devices such as complementary metal oxide semiconductor (CMOS). We have already reported the concept of parallel processor system with optical interconnection [4]. However, the coupling efficiency between waveguides and VCSELs/PDs was low due to the alignment error. To overcome these problems, we developed a new optical interposer with passive alignment using high performance polynorbornene (PNB) optical waveguide [5]. In this paper, we describe the fundamental properties of the optical interposer.

2. Passive alignment optical interposer

Figure 1 illustrates the configuration of parallel processor system. Three-dimensional (3-D) LSI chips with processor element are connected to each other by optical interconnections. Therefore, the high-speed I/O signal of 3-D LSI can be transferred among them through optical interconnection system. Figure 2 shows the cross-sectional structure of optical interposer. In this system, Si wafer instead of PCBs is employed as a substrate to achieve the optical alignment with high accuracy. This is due to using high-precision processing technology for Si such as micro electro mechanical system (MEMS). VCSELs and PDs are self-assembled with solder and buried into cavities photolithographically formed in a Si wafer. Therefore, the optical windows of laser emitting apertures and PD are precisely aligned at the designed points. Consequently, passive optical alignment can be achieved with the standard LSI equipments. In addition, the gap between optical waveguide and VCSELs/ PDs is minimized because the PNB optical waveguide is fabricated on the Si wafer. Furthermore, the PNB optical waveguide has very low optical loss with 0.03 dB/cm at a wavelength of 850 nm. These advantages can decrease the coupling loss and the insertion loss. Therefore, any additional optics such as a micro-lens are not required. In this paper, we report the test module fabrication of the optical interposer with cavities and VCSELs/ PDs. Figure 3 shows the fabrication process for the test module of the optical interposer. First, silicon dioxide (SiO_2) was deposited on a Si wafer by chemical vapor deposition (CVD). The SiO_2 layer acts as an insulator and also a sacrificed layer for forming electrical pads on the cavities. Second, the 10-nm-thick Ta and the 500-nm-thick Cu was spattered on the SiO_2 layer. Third, the electrical circuit was pattened by photolithography. Next, the Si was etched from the backside to form deep cavities by inductively coupled plasma reactive ion etching (ICP-RIE) using the Bosch process. After that, PNB optical waveguide was fabricated on the SiO_2 layer and the electrical circuits. Next, sacrificed SiO_2 layer of cavities was removed by wet etching. Finally, VCSELs/ PDs were buried into the cavities and 45^o mirrors were formed by an excimer laser.

3. Experimental Results and Discussion

The pattern size of cavities was designed only 15 μm bigger than that of VCSELs and PDs. This design prevents VCSELs and PDs from shifting, inclining and rotating. Figure 4 shows the cross-sectional view of a resulting cavity. Si etching was stopped at the SiO_2 surface because the etching selectivity of Si/SiO_2 is about 200/1, and thus, cavities were uniformly formed on the overall Si wafer. As a result, the depth of the cavities can be kept constant at everywhere on the Si. The cavity sidewall without tapered profile was clearly observed as shown in Fig.4 (a) and (b). Therefore, VCSELs and PDs can be easily loaded on the bottom of the cavities. The corner of the square patterns tends to round after photolithographic process, resulting in a critical defect for high-accuracy alignment using such cavities. The dependence of cavity corner designs on their shape after etching was estimated by using the five patterns as shown in Fig. 5 (a). Figure 5 (b) shows the photomicrographs of the resulting corner edge. As seen from Fig.5, the pattern number a-4 can nearly produce square shape of the cavity corner. PD was buried in the resulting cavity as shown in Fig. 6. Figure 6 (a) illustrates a diagram describing the dimension and layout on a buried PD as seen in Fig.6 (b) which shows the photomicrograph of the top view of the fabricated cavity with the PD after removing sacrificed SiO_2 layer. Figure 6 (c) shows the cross-sectional view of a fabricated cavity with the PD. The

cavities, 495 μm on a side, were designed to have somewhat bigger size than PD with 480μm on a side. The location of laser emitting aperture was almost aligned onto the designed point.

The relationships between coupling losses and optical passes between 45° mirror and a VCSEL/ a PD were estimated. The experimental setup shows in Fig. 7. The waveguide was coupled to an 830-nm laser diode source using a 50-μm multimode fiber. At the output end, the transmitted light was coupled to a photodetector using a 100-μm multimode fiber and the power was measured using an optical power meter. As seen from Fig. 8, the characteristics of coupling losses using the optical interposer are improved and the loss was lower than the sample with 100 μm in optical pass we have previously fabricated. The loss decreased more than 1.5 dB.

4. Conclusion

We proposed a new optical interposer for a parallel processor system. We fabricated the test module of optical interposer with VCSELs/ PDs buried in the cavities. It is confirmed that the optical interposer can achieve the passive optical alignment using the standard LSI equipments. In addition, the coupling loss of this optical interposer without the micro-lens was improved -1.5 dB.

References

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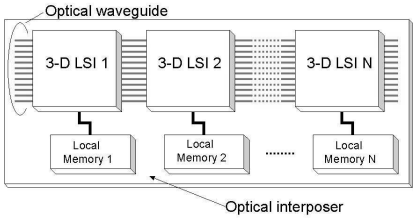

Fig. 1. Parallel processor system connected by optical interconnection.

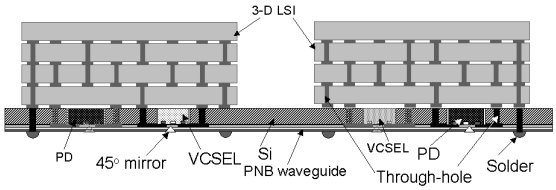

Fig. 2. Structure of optical interposer.

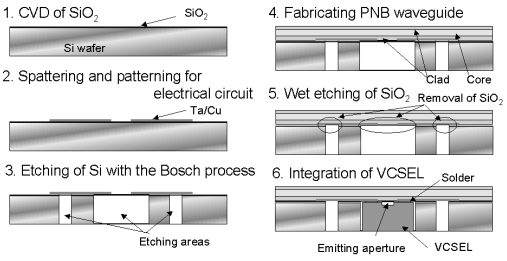

Fig. 3. Fabrication process for the test module of the optical interposer.

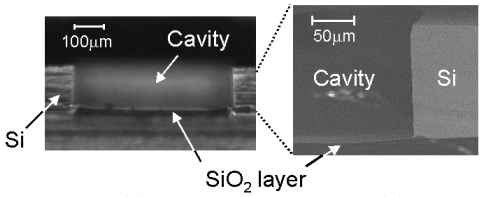

Fig. 4. Cross-sectional view of photomicrograph (a) and SEM micrograph (b) of resulting cavity

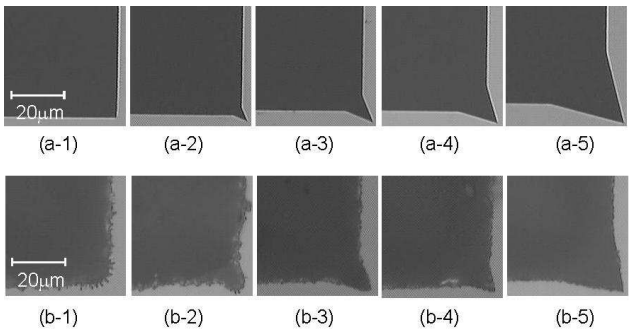

Fig. 5. Mask design of the corner for the cavity (a) and photomicrograph of the corner of resulting cavity after etching (b).

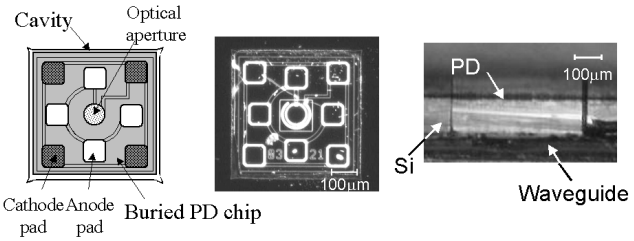

Fig. 6. Diagram of describing the dimension and layout on a buried PD (a), photomicrograph of top vie of fabricated cavity with the PD without sacrificed SiO_2 layer (b), and photomicrograph of cross-sectional view of a fabricated cavity with the PD (c).

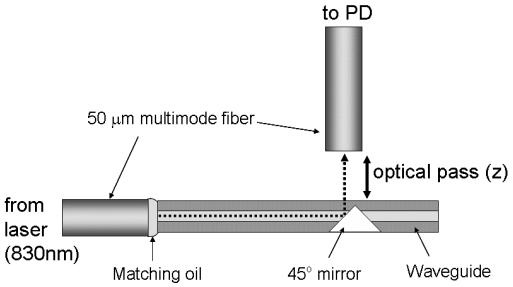

Fig. 7. Experimental setup for measurement of coupling loss.

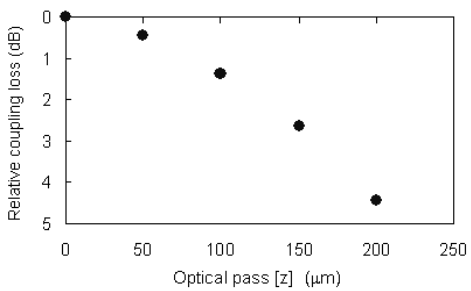

Fig. 8. The relationships between coupling losses and optical pass