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A Breakthrough Electronic Lithography Process Through Si Layer for Self Aligning Gates in Planar Double-Gate Transistors for 32nm Node And Below

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Abstract
We report here the first demonstration of aligning patterns through silicon layers thanks to high energy electron beam lithography. This novel process is a promising solution for self aligning gates in planar double gate devices integration.

1. Introduction and challenges

Thanks to its perfect channel electrostatic integrity, multi-gate transistor is considered as the best solution to reach ITRS specifications for the 32nm node and below [1]. Planar double gate transistor architecture is among one of the most promising ones [2]. The main challenge for this architecture is to define a bottom gate pattern under the channel while keeping channel integrity. Several options were discussed, including bonding [3], damascene integration [4] or additional lithography, etching and epitaxy in our previous work [5][6]. We introduce here a revolutionary process allowing us to perform lithography under thin layers. We achieved to self align patterns without additional process step except standard electronic lithography. Silicon channel integrity is kept unchanged. It consists of exposing resist on each side of Si channel using high energy electron beam. Integration scheme is associated using HSQ resist which is transformed into low-k dielectric after curing.

2. Electron Beam lithography through silicon layers

SELID [7] monte-carlo simulator shows electron trajectories in a silicon substrate for a 50 keV exposition (fig 1a). Lateral dispersion is mainly due to direct diffusion and back scattering. Nevertheless dispersion only occurs after few microns depth. Simulations have also been performed through three stacks above the substrate (fig 1b): 40nm HSQ (Hydrogen Silsesquioxane) resist on both sides of a 30nm silicon layer. It highlights electrons statistical deviation between the two HSQ/Si interfaces is less than 2nm. Therefore energy transfer through silicon layer is anisotropic for thin films. We fund an innovative way to self-align patterns on both sides a planar layer.
Morphological demonstration has been done using conventional electron beam lithography (EBL) tool at 100 keV. Process follows these steps: After an epitaxial growth of a SiGe/Si bilayer, we realized an anisotropic etching of the stack to access laterally to SiGe. Isotropic partial etching of SiGe is then realized thanks to conventional SON process [8]. This results with a silicon bridge hanged up by SiGe pillar (fig 2a, fig 3). HSQ resist is spin-coated (2b) over and under silicon layer. Fig 4 shows torn-up silicon after cleaving, pointing out HSQ in cavities. It demonstrates the ability of HSQ to be spin-coated in a 40nm thick tunnel and its perfect conformity. The following step is electron exposure (fig 2c). Then HSQ is developed thanks to a TMAH based solution (fig 2d). This results with HSQ surrounding silicon layer (fig 5). TEM view of the structure after development can be seen fig 6. High Critical Dimension (CD) control is demonstrated. Top and bottom patterns are 78nm and 80nm width respectively. Patterns are exposed through a 16 nm mono-silicon layer. Note perfect crystallinity of silicon is conserved. This view confirms simulation results.

3. Double Gate device integration using HSQ resist

HSQ is a spin coatable oxide which is also a negative tone electron beam resist. During curing, or electron exposure, its cage-like structure $(HSiO_{3/2})_{2n}$ is opened, and forms a network structure (polymerization) [9]. It leads to a low-k dielectric, similar to SiO_2. Then, as opposed to conventional resists, HSQ can be part of a front end process as a dielectric. HSQ combined with first described high energy EBL process is a way to form a dummy gate or its opposite pattern: Both direct [5] or damascene [4] integration can be considered.
One proposal is explained fig7: HSQ is spin coated on each side of a silicon bridge. High energy electron beam lithography is performed, and non exposed HSQ is developed. Conform nitride is deposited (including in the cavities) and planarized thanks to CMP process [10]. HSQ is totally etched selectively versus nitride. The following step is the filling of former HSQ pattern with gate stack using CVD or ALD process

and planarization of the stack over nitride. Then nitride is totally removed. End of the process is a standard thin film one: spacers, implants, salicidation and back end.

4. Conclusion

We demonstrate in this work a revolutionary way to integrate multi gate devices using standard electron beam lithography. Considering resolution potential of EBL combined with HSQ below 20nm [11], studies about EBL high throughput [12] comprising multi-beam tools [13], Electron Projection Lithography [14], this solution can be considered as a serious candidate for CMOS 32nm node and below.

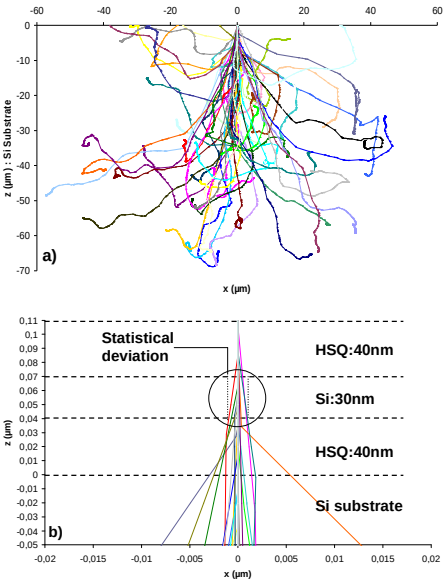


Fig1 : Monte Carlo simulation of electron trajectories @100keV a) in substrate b) through Si layer between two HSQ resist films.

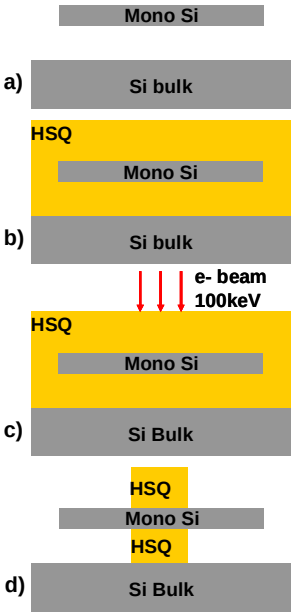


Fig2: Sequence of Electron Beam lithography through thin Si layer.

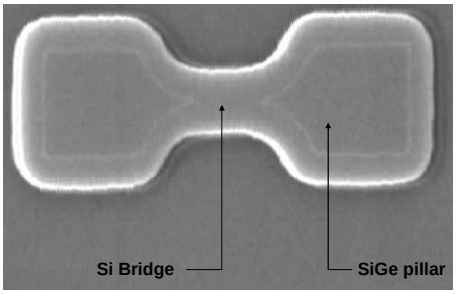


Fig 3: High Energy SEM top view of a silicon layer hanged up by SiGe pillars.

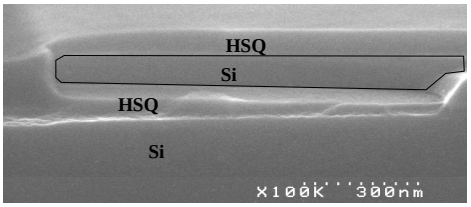


Fig4:Conformity of HSQ deposition in cavities.

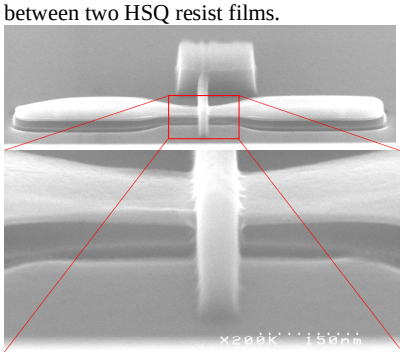
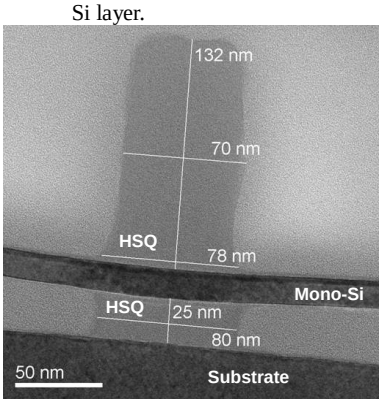


Fig5:HSQ dummy gate aroud silicon bridge.



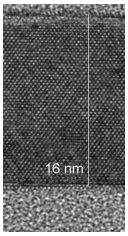


Fig6: TEM view of twin HSQ pattern on both side of Si layer.

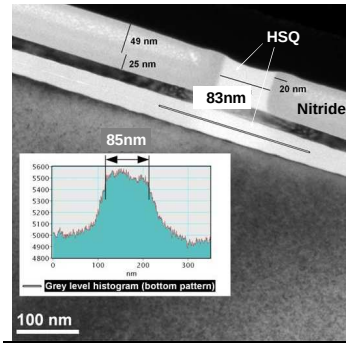


Fig8: TEM view of nitride planarization step (fig7d)

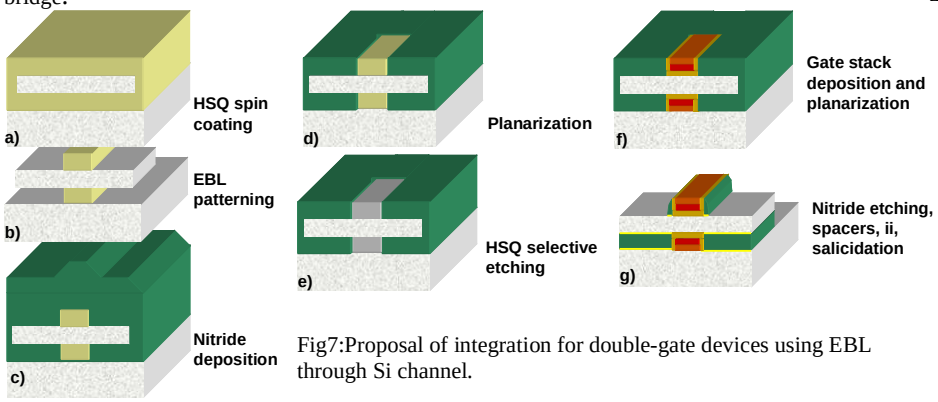


Fig7:Proposal of integration for double-gate devices using EBL through Si channel.

References :

[1] International Technology Roadmap for Semiconductors 2005.
[2] S.Harrison et al., IEDM Tech Dig, 2003, p449
[3] J.Widiez et al. SOICONF 2004.
[4] S.Y Lee, Symp VLSI tech 2004, p. 200.
[5] R.Wacquez et al, SSDM proc p534.
[6] A.Pouydebasque et al., SNW2007.
[7] SELID SIGMA-C manual utilisator
[8] S.Monfray et al., IEDM Tech 2001, p645.
[9] HC.Liou et al., Thin Solid Films 335 (1998) p186-191.
[10] F.van Delft et al., J.Vac.Sci.Technol B 24(6) p3125, 2006.
[11] J.Kretz et al., Micro.Eng vol78-79, 2005.
[12] L.Pain et al., CR Physique 7 (2006)
[13] MJ van Bruggen et al., J.Vac.Sci.Technol B (23)6, 2005
[14] M.Yamabe et al., J.Microlith.Microfab.Microsyst 4(1), 2005.