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Contact Technology employing Nickel-Platinum Germanosilicide Alloys for P-Channel FinFETs with Silicon-Germanium Source and Drain Stressors

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1. INTRODUCTION

Integration of lattice-mismatched SiGe S/D stressors for p-channel FinFETs has realized devices with enhanced drive currents [1], [2]. To reap the full benefits of channel strain engineering, it will be imperative to realize compatible low resistance S/D silicides on SiGe. This is especially crucial for FinFETs as the formation of narrow Si-fins with low series resistance is a primary integration challenge [3], [4]. Although nickel-germanosilicide (NiSiGe) is compatible with SiGe S/D technology, agglomeration has been observed to occur at low processing temperatures due to the enhanced out-diffusion and segregation of Ge in narrow line-widths [5]. This renders morphological instability of NiSiGe an important issue for aggressively-scaled CMOS technologies. Alloys of Ni(Pt)SiGe have been investigated to engineer a more robust NiSiGe film [6]. To date the integration of Ni(Pt)SiGe has been demonstrated only for planar device architectures with an undisclosed Pt concentration [5].

In this paper, we investigate the material and electrical characteristics of NiSiGe with Pt concentrations up to 20 atomic % (at. %), as determined by Rutherford backscattering. An optimum Pt concentration in NiSiGe with a suitably low sheet resistivity and Schottky-barrier height (SBH) was selected for integration in p-channel FinFETs. This work also reports the first integration of nickel platinum germanosilicides in strained p-channel FinFETs with SiGe S/D regions.

2. EXPERIMENTAL SET UP

10 nm thick Ni and Ni(Pt) alloy films with different Pt at. % (5, 10, and 20) were sputter deposited on dilute-HF cleaned epitaxially grown $S_{i0.74}Ge_{0.26}$ films on n-type Si(001) substrates for materials characterization. The samples were subjected to a two-step rapid thermal anneal (RTA) process (320 ^{o}C, 60s followed by 350-700 ^{o}C, 30s) in nitrogen. Selective metal removal was completed using a sulphuric-acid-hydrogen-peroxide solution, H_2SO_4:H_2O_2 [4:1] at 120 ^{o}C for 60s.

3. RESULTS AND DISCUSSION

A. Material Characterization

Sheet resistivity (ρ_{sheet}) transformation curves in Fig 1(a) reveals that the addition of Pt increases ρ_{sheet} by about 16 % at 400^{o}C independent of Pt concentration. The dramatic increase in ρ_{sheet} for NiSiGe films at temperatures $\geq$ 550^{o}C is attributed to Ge out-diffusion that leads to agglomeration. The onset of morphological instability occurs at 500^{o}C for pure NiSiGe films (thickness~22nm), as indicated by the 44% degradation in ρ_{sheet} performance compared to NiSiGe films RTA at 400 ^{o}C [Fig. 1(b)]. On the other hand, ρ_{sheet} values for the Ni(Pt)SiGe systems remain relatively stable. Fig. 2 shows the current-voltage (*I-V*) characteristics of NiSiGe and Ni(Pt)SiGe Schottky diodes annealed at 450 ^{o}C. Well-behaved *I-V* characteristics were observed for all diodes [Fig. 2(a)] except for the diodes fabricated with Ni(Pt20%)SiGe, which exhibits a wide distribution in the reverse current [Fig. 2(b)]. We speculate that Ni(Pt)SiGe metal silicidation with Pt concentrations > 10 at. % induces electrically-active defects in the junctions [7]. SBHs of 0.678 eV, 0.769 eV, 0.811 eV, and 0.775 eV were extracted for diodes fabricated with NiSiGe, Ni(Pt5%)SiGe, Ni(Pt10%)SiGe, and Ni(Pt20%)SiGe, respectively, using a thermionic emission model [Fig. 3]. It was found that Ni(Pt10%)SiGe possess the largest SBH of 0.81eV with an ideality factor (n) = 1.008. The increase in n for diodes with Ni(Pt20%)SiGe indicates an appreciable increase in the recombination currents. This observation supports our speculation that Ni(Pt)SiGe metal silicidation with Pt concentration >10 atomic % induces electrically-active defects in the junctions. By considering tradeoffs between ρ_{sheet} and SBH, we selected Ni(Pt10%)SiGe for subsequent material analysis and device integration in this work.

SIMS analysis shows a varying distribution of Pt within the bulk NiSiGe film with a minute amount at the NiSiGe-Si interface after 450 ^{o}C RTA [Fig. 4(a)]. This leads us to conclude that NiSiGe SBH modulation achieved with Pt addition is due to a change in intrinsic metal work function instead of Pt segregation at the interface. XRD analysis shows the presence of only a single phase of Ni(Pt)SiGe mono-germanosilicide at 450 ^{o}C, indicating 10 at. % Pt does not affect the phase formation kinetics of NiSiGe. By comparing plan-view SEM images for NiSiGe and Ni(Pt10%)SiGe films it becomes evident that 10 at. % Pt is sufficient to suppress agglomeration of NiSiGe films at elevated temperatures [Fig. 5]. Cross-sectional TEM in Fig. 6 confirms the superior morphological stability of Ni(Pt10%)SiGe at higher RTA temperatures. Severe grain boundary grooving resulting in voids can be found for NiSiGe films RTA at 700 ^{o}C. In contrast, a continuous void-free Ni(Pt10%)SiGe film is present after 700 ^{o}C RTA. The suppression of agglomeration with Pt addition is attributed to reduced grain boundary energies and the increase in surface and interface energies of Ni(Pt)SiGe films [8].

B. Device Characterization

We have integrated Ni(Pt10%)SiGe into a standard FinFET process flow [2] with selective epitaxy growth of SiGe S/D stressors [Fig. 7(a)-(c)]. A cross-sectional TEM image of a p-channel FinFET shows the successful formation of Ni(Pt10%)SiGe in the SiGe S/D regions [Fig. 8]. Fig. 9 shows the I_{DS}-V_{GS} characteristics of two closely matched devices with similar Off-current, DIBL (0.03V/V), and subthreshold swing (90 mV/decade). FinFETs with Ni(Pt10%)SiGe S/D silicide shows 18% higher I_{Dsat} than FinFETs with NiSiGe S/D silicide [Fig. 10]. I_{Dsat} enhancement is attributed to the improved surface/interface morphology [Fig. 5 and 6] and reduced series resistance [Fig. 11].

4. SUMMARY

In summary, we explored the material and electrical characteristics of NiSiGe films with different Pt concentrations. A superior Ni(Pt)SiGe film with an optimized Pt concentration to provide suitably low ρ_{sheet} and SBH was engineered. In addition, the first demonstration of specifically engineered germanosilicides for p-channel FinFETs to address integration challenges for aggressively-scaled CMOS devices is presented.

References

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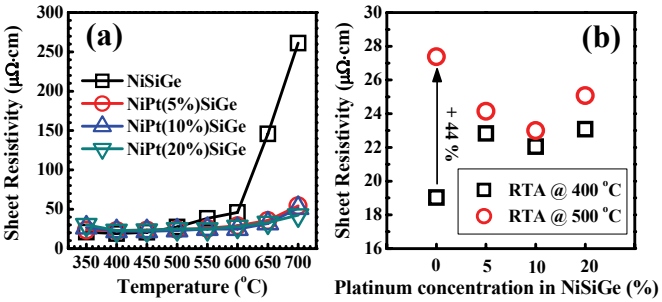

Fig. 1. (a) ρ_{sheet} transformation curves for NiSiGe with different Pt concentrations. (b) Typical ρ_{sheet} values for NiSiGe with different Pt concentrations annealed at 400 and 500 °C. Significant increase in ρ_{sheet} observed for pure NiSiGe films when annealed at 500 °C.

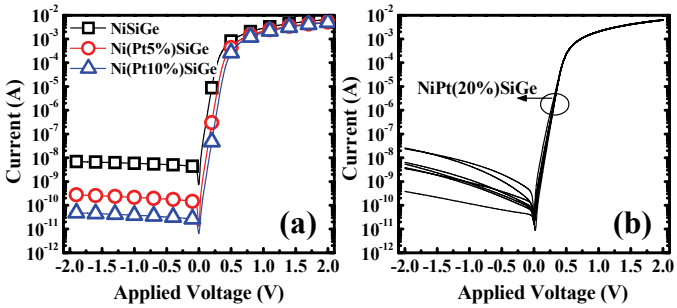

Fig. 2. *I-V* characteristics for Schottky diodes formed on epitaxially grown $Si_{0.74}Ge_{0.26}$ on n-Si(001) substrates annealed at 450 °C. (a) Typical *I-V* curves for NiSiGe, Ni(Pt5%)SiGe and Ni(Pt10%)SiGe diodes. (b) *I-V* curves for Ni(Pt20%)SiGe diodes show a wide distribution of reverse currents.

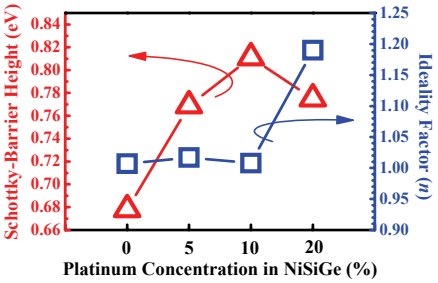

Fig. 3. Extracted SBHs and *n* for different Pt concentrations in NiSiGe using the thermionic emission model. Increase in *n* was observed only for Ni(Pt20%)SiGe diodes.

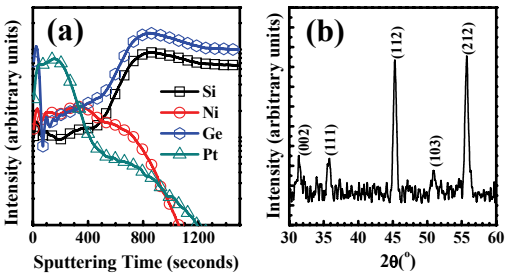

Fig. 4. (a) SIMS depth profile for Ni(Pt10%)SiGe films annealed at 450 °C shows the distribution of Pt in the bulk silicide region. (b) XRD shows the presence of a single phase for Ni(Pt10%)SiGe films annealed at 450 °C.

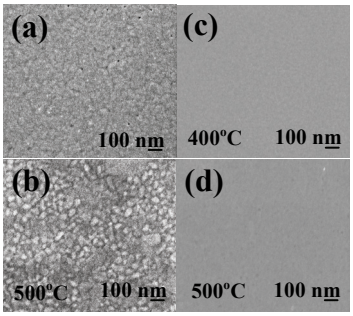

Fig. 5. Plan-view SEM micrographs for NiSiGe and Ni(Pt10%)SiGe films annealed at 400 and 500 °C. (a)-(b) NiSiGe and (c)-(d) Ni(Pt10%)SiGe.

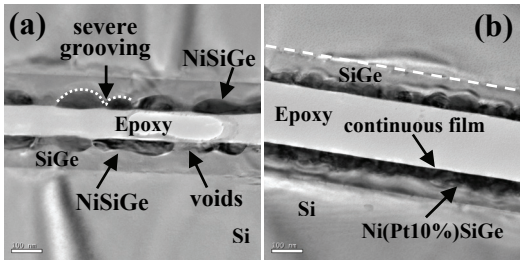

Fig. 6. TEM images for films annealed at 700 °C. (a) NiSiGe films reveal severe grain boundary grooving and the formation of voids. (b) Addition of 10 at. % of Pt suppresses film agglomeration and the formation of voids. Grain size is ~100-150 nm. Note: Each TEM image has two film samples by using epoxy to adhere two film surfaces together during TEM sample preparation.

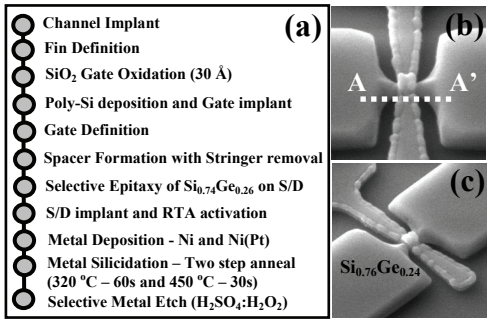

Fig. 7. (a) Process sequence employed in the fabrication of FinFETs with SiGe S/D stressors. (b)-(c) Tilt-SEM images showing a FinFET with SiGe (~60nm) stressors grown selectively on the S/D regions.

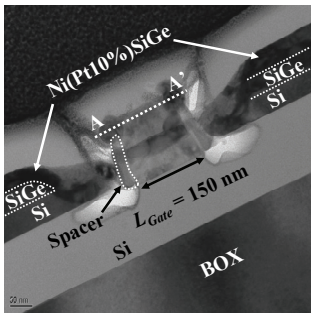

Fig. 8. TEM image of a FinFET with 150 nm poly-Si gate and Ni(Pt)SiGe S/D silicide. Note: FIB cut was along the A-A' plane, which overestimates the L_G [Fig. 7(b)].

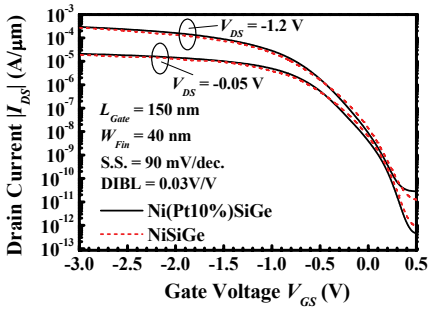

Fig. 9. I_{DS}-V_{GS} characteristics of FinFETs with NiSiGe and Ni(Pt10%)SiGe exhibits similar OFF-current, DIBL and subthreshold swing. This indicates that Pt addition does not have a detrimental impact on the device subthreshold characteristics.

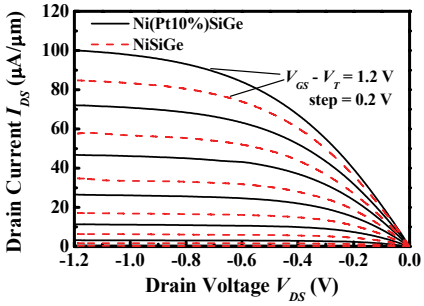

Fig. 10. I_{DS}-V_{DS} characteristics of FinFETs with Ni(Pt10%)SiGe S/D silicide exhibits a 18% saturation drive current enhancement compared to FinFETs with NiSiGe S/D silicide. This is attributed to lower series resistance and improved film morphology.

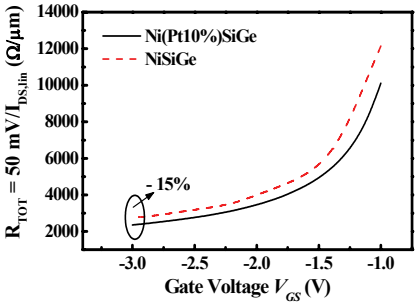

Fig. 11. Extraction of series resistance by examining the asymptotic behavior of total resistance at large gate bias. FinFETs with Ni(Pt10%)SiGe S/D silicide have a lower R_{TOT} compared to FinFETs with NiSiGe S/D silicide attributed to the lower SBH of Ni(Pt10%)SiGe.