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An Optimized Silicidation Technique for Source and Drain of FINFET

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1. Introduction

Three-dimensional (3-D) devices e.g. FinFET [1, 2], have been extensively developed for further scaled devices. Suppression of short-channel effects can be realized on these device structures, but, drive-current decrease by parasitic resistance is caused. Figure 1 shows simulated I_D-V_G characteristics of devices with different two contact structures [3]. This result shows that parasitic resistance of source and drain, S/D causes driving-current decrease for top-contact structure device. To overcome this problem, it is needed to form low-resistive S/D. From this viewpoint, a Ni-silicidation technique for vertical S/D is investigated.

2. Experimental

For the case of 3-D structure devices, there are some issues on silicidation process. Figure 2 shows a cross-sectional view of Ni film deposited by sputtering method at 200 ^{o}C. Directionality of the sputtering causes deposition-rate difference between horizontal and vertical surfaces. As a result, there is surplus metal on horizontal surfaces. After silicidation annealing in deposition chamber at 450 ^{o}C in situ, deformation of Si patterns is observed as shown in Fig. 3. It is noted that the degree of these deformation depends on its pattern width [4]. These results show that each amount of Si and Ni influences silicide formation. To avoid these phenomena, deposition of appropriate amount of Ni and sensitive control of annealing conditions are needed.

Pressure dependence of deposited Ni thickness on vertical sidewall is shown in Fig. 4. Its thickness uniformity is improved as the deposition pressure becomes larger. The thickness ratio, $t_{side/top}$ achieves 0.38 at 0.75 Pa when the thickness on horizontal surface is 100 nm. This condition is adopted in this work. When thicker Ni film is needed on the sidewall, a chemical-vapor deposition, CVD has much better potential to obtain conformal deposition [5]. To exclude the influence of the temperature change when a sample is heating, silicidation annealing is carried out during deposition.

3. Results and discussion

Figure 5(a) shows an SEM image of a Si beam silicided by in-situ annealing at 300 ^{o}C. 55-nm-thick Ni-silicide film is uniformly formed on the sidewall, but silicide formed by Si-diffused reaction is observed at the edge of patterns. This result shows that the shape of Ni silicide changes sensitively in each part of vertical structure. For the case of 250 ^{o}C annealing shown in Fig. 5(b), deformation caused by Si diffution is suppressed and 30-nm-thick silicide film is formed. XRD spectra for these samples are shown in Fig. 6. Ni_3Si_2 phase is observed as a dominant peak at 300 ^{o}C-annealing case, but deformation of Si beam is occurred in this case. For 250 ^{o}C-annealing case, Ni richer film, Ni_2Si phase is detected, and Si-beam deformation caused by Si-diffused reaction is not observed. After annealing at 250 ^{o}C and unreacted Ni removal by SPM, NiSi film is obtained by rapid thermal anneling at 450 or 500 ^{o}C avoiding Si-beam deformation.

Figure 7 shows an SEM image of a Si beam silicided by two-step annealing process. 60-nm-thick NiSi film is uniformly formed on the sidewall without abnormal deformation of Si-beams.

4. Summary

A Ni-silicidation technique of source and drain for FINFET has been discussed. For devices with 3-D structure, it is important to provide appropriate amount of Ni and to control annealing conditions for avoiding abnormal deformation of Si beams. In this work, surplus Ni deposition on the horizontal surface is decreased by deposition-pressure control. In addition, a silicidation annealing carried out during deposition is adopted to exclude the influence of the temperature change when a sample is heating.

Si-diffused reaction causes deformation of Si-patterns in cases of annealing at 300 ^{o}C or higher. A two-step annealing process prevents this phenomenon and NiSi film is uniformly formed on vertical walls without abnormal deformation.

Acknowledgements

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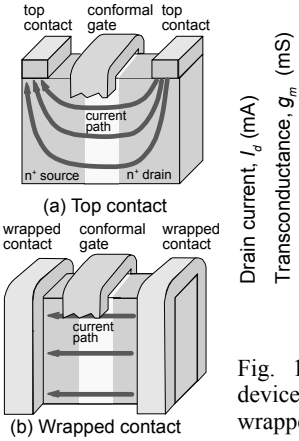


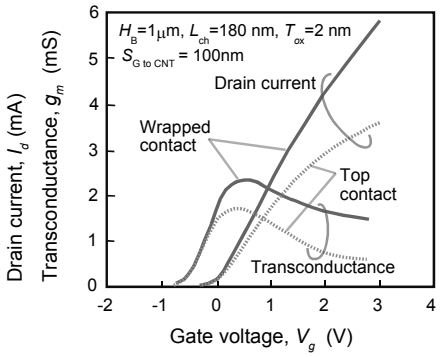


Fig. 1 Simulated I_D-V_G characteristics of devices with usual top contact, (a) and wrapped contact, (b).

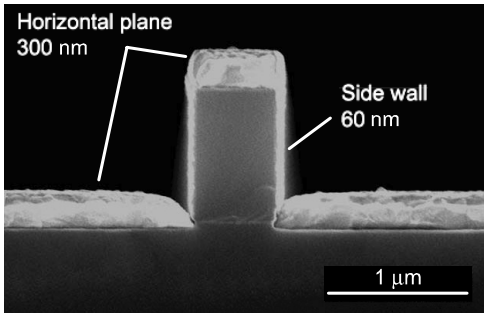
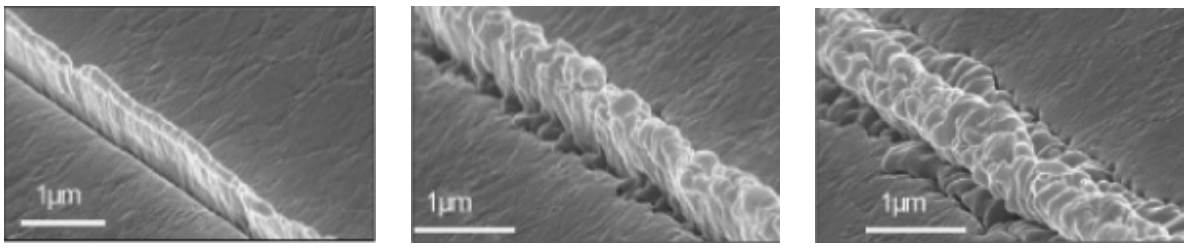


Fig. 2 An SEM image of deposited Ni film on vertical Si wall by sputtering method.



(a) W_B = 150 nm (a) W_B = 300 nm (a) W_B = 500 nm

Fig. 3 Bird's eye views of Si beams silicided in deposition chamber at 450 °C. The degree of these undesirable deformations depends on its pattern width [4].

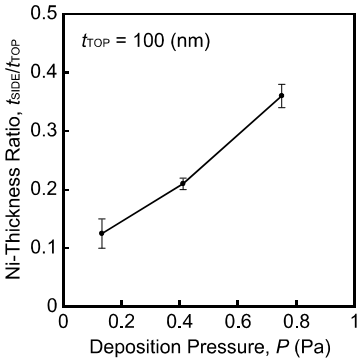
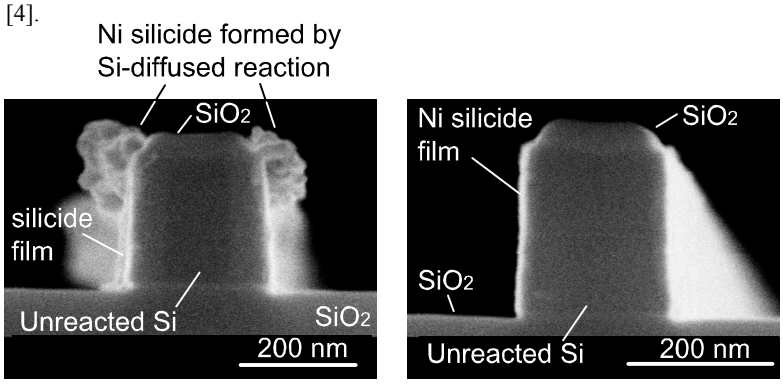


Fig. 4 Pressure dependence of Ni thickness deposited on the sidewall when the thickness on horizontal surface is 100 nm.



(a)300 °C (b) 250 °C

Fig. 5 Silicided beams formed at 300 and 250 °C. In the former condition, Ni silicide formed by Si-diffused reaction is observed.

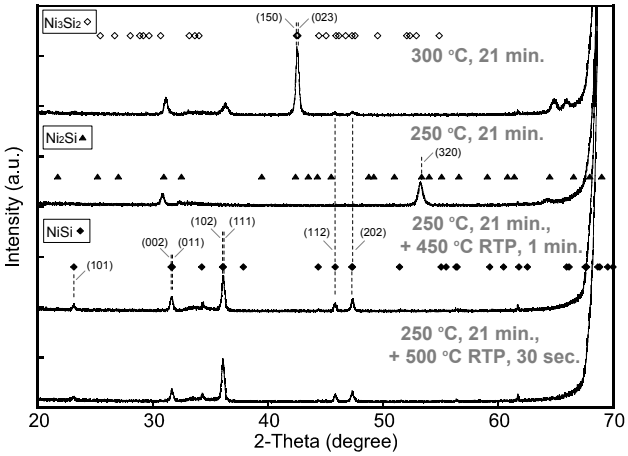


Fig. 6 XRD spectra of silicided samples annealing at 300, 250 °C and two-step annealing.

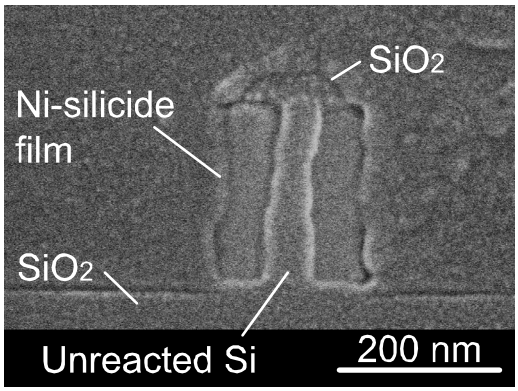


Fig. 7 A cross-sectional view of Ni-silicided beam formed by two-step annealing process.