A Novel Approach to Fabricate ~120 nm Thick Fully Relaxed Ge-on-Insulator

S.Balakumar,^{a)} K.M.Hoe, W.Tang, Y.L.Foo[†], S.Tripathy[†], C.H.Tung, G.Q.Lo, N.Balasubramanian and D.L.Kwong Institute of Microelectronics, 11 Science Park Road, Science Park II, Singapore-117685, †Institute of Materials Research and

Engineering, 3 Research Link, Singapore 117602, ^{a)} Email: <u>subra@ime.a-star.edu.sg</u>.

1. INTRODUCTION

Monolithically integrated photonics, with CMOS for optoelectronic applications, is gaining interest for either adding new functionality to the electronic circuits or minimizing circuit block for optical telecommunications [1, 2]. Presently crystalline or polycrystalline Ge-on-Si have been proposed for detector device for wavelength at 1.5µm. However, Ge-oninsulator (GOI) or high-Ge-content SiGe-on-insulator (SGOI) are the selected options for photonics because of both bulk Ge properties and "on-insulator" advantages. Many ways to achieve the SGOI/GOI have been demonstrated [3]. Ge condensation [4] is a potential technique to fabricate small and large substrates. However, there are many challenges and issues [3]. Previously, we reported issues such as Ge ball-up, SiGe amorphization, and SiGeO formation/oxidation termination; meanwhile, also reported the effectiveness of a modified condensation process for thin SGOI to circumvent such [4-9]. However, it is very difficult to achieve such for a thick film (e.g., ≥ 100 nm) by the condensation due to the required longer duration and issues from oxidation saturation [9]. To reduce the required temperature and time, we further developed a refined approach. In this paper, we present a novel way to achieve high Ge content relaxed GeOI for the first time. Defect formation, in plane strain and oxidation saturation issues of the formed layers are investigated in detail.

2. EXPERIMENTALS

For starting substrate, Si-on-Insulator was thinned down to \sim 170Å using thermal oxidation. About 12 -150 nm Ge was deposited with \sim 12 nm grading layer in UHVCVD chamber at temp at 550°C. 200 to 900 thick SiO₂ was deposited as cap-layer on top of the stack to avoid Ge-loss during annealing and also to control the condensation rate. Two-steps or single-step annealing methods are used to mix it. Then the film was condensed in pure O₂ at 950°C and below. SGOI layers were characterized using HRTEM, X-ray diffraction, and micro-Raman analysis.

3. RESULTS AND DISCUSSIONS

Fig.1 illustrates the schematic representation of thermal mixing and condensation approach. The deposited oxide cap-layer over



Fig.1: Schematic of High SiGe growth /graded SiGe layer/SOI, intermixing and condensation approach

The stack helps to control the oxidation by controlling the amount of oxygen (O_2) radicals reaching SiGe/Oxide interface in addition to preventing the loss of Ge during oxidation and annealing. As-grown SiGe on thin graded SiGe has high defect count and the Ge content is ~97% as shown in Fig.2 (a). First, a two-steps annealing at 750°C and 800°C with 1hr each cycle resulted in SGOI film with [Ge]~72% but still some defects such as dislocation lines and stacking fault can still be seen in

parallel to the 60° line defects (Fig.2(b-c)). One-step anneal at 850°C for 3 hrs drastically reduced the defect amount and improved the Ge uniformity across the film. The SiGe layer thickness was ~1600Å. One-step anneal at high temperature is thus sufficient to achieve low defect layer. Utilizing this method, we achieved less defective $Si_{0.28}Ge_{0.72}OI$ layer without issue as compared to the two-steps anneal step. <u>This seems to be an easier way to achieve high Ge content among all techniques so far.</u>

Subsequently, Ge condensation was carried out at oxidation at 950°C for 30 min with intermittent annealing. The Ge content was increased to 80%. In previous thin SGOI film fabrication [7], the condensation temperature was reduced to 900°C when the Ge content became \geq 60%. In this work, since we used thick oxide as the cap-layer, oxidation has been carried out at higher temperatures to diffuse more oxygen through to reach to oxide/SiGe interface.



Fig.2: TEM image of the epitaxially grown SiGe layer on SOI with graded layer.



Fig.3: TEM images of thermally mixed layer. Insets (b) and (c) show the defects and stacking fault formed during mixing

Therefore, condensation was carried out at 950°C until Ge reached ~80%. Then the second step condensation temperature was reduced to 900°C. Adequate intermittent annealing was given to ensure that Ge spreading across the thick layer to prevent over oxidation and SiGeO formation [7]. Fig. 3 shows the thick Ge layer and the thickness is ~1200Å. HRTEM studies indicate the formation of high quality GOI as shown in Fig. 3(b).



Fig.4: (a) TEM images of condensed Ge layer, (b) HRTEM picture which does not have defects



Fig.5: Raman spectra of SGOI samples with different Ge contents.

MICRO-RAMAN AND X-RAY DIFFRACTION: For strain measurements in Ge-rich SiGe films with Ge composition x>0.5, the strain is directly calculated from the frequency-shift of Ge-Ge mode with respect to the phonon peak of the bulk SiGe (strain-relaxed) with the same Ge composition. For 80% and 100% of Ge in strain-free bulk SiGe, the unstrained values of the Ge-Ge phonon frequencies appear around 296 and 300 cm⁻¹, respectively. Our results show that Ge-Ge mode appeared at 296.2 and 300 cm⁻¹ for the cases of 80% and pure Ge contents in SGOI films as shown in Fig. 5. Both layers were found to be fully relaxed. For further confirmation, HRXRD analysis (Fig.6) was carried out for GeOI. The lattice constant of the system, calculated from the reciprocal space map, is 5.658 Å. Since lattice constant for out of plane is also similar, it is thus confirmed that the film is pure Ge and is fully relaxed.



SATURATION OXIDATION **PHENOMENON:** The condensation started at 950°C with considerably thick (900Å) oxide layer on top of SiGe layer. The oxidation saturation was found to take place once the oxide thickness was increased to ~1100Å, though the Ge content was 80%. It has been proposed previously that the possible origins for oxidation saturation phenomenon could be due to the strain in the SGOI layer [4], and the increase of Ge fraction near the interface [8]. However, the exact role of oxide layer was not clear. In our earlier studies, we did not come across the self-limiting oxidation even with 3000Å thick oxide layer formed as the SiGe being thinned down to 300Å [7]. But in such cases, when the oxide thickness increased to ~1200Å, the SiGe thickness reduced to 1200 Å but the Ge content was still less than 25% [6]. In this work, the SiGe layer thickness is ~1445 Å and the oxide thickness was ~1100 Å and we should note that Ge content is >70%. Oxidation saturation occurred only when the thickness of the SiGe layer is >1000Å with Ge content above 40% provided the top oxide layer should be >1100 Å. Since the oxide layer is stressed due to the bottom layer, oxygen radical couldn't diffuse toward the interface. It confirms that, the SiGe and oxide layers thicknesses and theirs stress relations are key factors. Based on the observed results, we predict that besides the SiGe thickness and accumulated stress, the oxide layer stress is also an important factor. In addition, if we increase the temperature from 950°C to 1000°C, oxygen radicals can diffuse down to oxidize the bottom layer. However, its extension has certain limit before saturation again occurs. It is found that all the factors such as SiGe and oxide layers thicknesses, Ge content in SiGe, the temperature, are playing critical roles in oxidation saturation and termination. Further details will be presented with more experimental data.

4. CONCLUSION

We have demonstrated a simple cost-effective way to fabricate thick *high Ge content SGOI/GOI* substrates by thermal mixing and condensation technique. X-ray diffraction and Raman studies confirmed that the layer is *full relaxed* GOI. Oxidation saturation depends on layers thicknesses and Ge content. This is novel and cost effective approach to fabricate 200mm and 300mm GOI substrates. It can also be co-integration applications since thermal cycle time can be very short. **References:**

- 1. J.M. Fedeli et al, ECS Transactions, v 3(7),p 771, 2006.
- 2. S.J. Koester et al, IEEE J. of Quantum Elec., 12 (2006)
- 3. V.Terzieva et al, ECS Transactions, v 3, p 1023 (2006).
- 4. T. Tezuka et al, Jpn. J. Appl. Phys, Part I, 40 2866 (2001)
- 5. M. M.-Roy, et al, 2005 SSDM, pp.368, (2005)
- 6. S. Balakumar et al, Appl. Phys. Lett. 89, 042115, (2006)
- 7. S. Balakumar et al, Appl. Phys. Lett. 90, 032111 (2007)
- 8. T. Shiumra et al Appl. Phys. Lett., 89, p 111923-1 (2006)
- 9. S. Balakumar et al, Appl. Phys. Lett. 90, 192113 (2007)