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A Novel Process-Compatible Floating Channel Crystallization Technique to Fabricate High-Performance Poly-Si TFTs

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1. Introduction

Solid-phase crystallization (SPC) of amorphous silicon (a-Si) has been attracted many interests for the application of polycrystalline silicon (poly-Si) thin-film transistors (TFTs) in active-matrix-liquid-crystal displays (AMLCDs) [1]. The performance of TFT is strongly dependent on the microstructure of poly-Si film. In particular, grain boundaries and intragranular defects which act as scattering centers and midgap traps are known to affect the carrier transport properties. To date, various techniques were proposed to improve the crystallinity of SPC poly-Si film [2]-[5]. Among those methods, a novel surface-nucleation SPC scheme, in which the nucleation started from upper a-Si surface, was proposed to significantly increase the grain size and to reduce the intragranular defects. In contrast, a interface-nucleation SPC scheme was known to get smaller grain. However, the proposed methods required complicated processes and are not practical for TFT application. Recently, Bo et al. [6] have proposed that SPC of suspended a-Si film, where the underlying silicon oxide (SiO_2) was removed prior to the crystallization would lead to larger grain size and lower intraguanular defects density.

In this paper, we introduced this novel crystallization scheme into the fabrication of high-performance floating channel TFTs (FC TFTs) with easy fabrication and self-aligned process for the first time. The FC TFT indeed reveals much improved performance over conventional TFTs (CN TFTs).

2. Experimental

The proposed FC TFT structure is schematically shown in Fig. 1. First, a 150-nm SiN_x, a 20-nm buffered SiO_2, and a 50-nm a-Si were successively deposited by CVD system on 6 in. Si wafers. After definition of the a-Si active region, a fluorine-based etchant was used to overetch the underlying buffered SiO_2 to make sure an air gap formed under the suspended a-Si channel as shown in Fig. 1(a), which we name floating channel. A SPC annealing was performed to transform a-Si into poly-Si. Next, a 100-nm TEOS oxide was deposited and a 150-nm poly-Si was deposited and patterned to be gate electrode as shown in Fig. 1(b). Self-aligned source and drain implantation, passivation oxide, dopant activation, contact holes, metal pads were successively performed. A NH_3 plasma was performed at 350°C for 30 min. For comparison, CN TFTs with underlying SiO_2 were also prepared with the same process as shown in Fig. 1(c).

3. Results and Discussion

The SEM image for FC and CN poly-Si film are shown in Fig. 2. The image obviously indicates that a better crystalline poly-Si with larger grain size and lower intragranular defect can be obtained in the FC poly-Si film. The TEM image for FC structure is also shown in Fig.3 with apparently an air-gap formed underneath the channel region. Typical I_D-V_G and I_D-V_D characteristics for FC and CN TFTs are shown in Figs. 4 and 5, respectively. The key device parameters are summarized in Table 1. Obvious performance improvements are acquired for FC TFTs. The main reasons for the superior performance are as follows: The rearrangement of Si atoms and volume contraction during SPC process will produce tensile stress in the Si films. Crystalline defects (microtwins, dislocation, etc.) must be generated to relieve the stress and a large number of nucleation sites are formed in CN poly-Si film. In contrast, since the Si atoms are completely free from the interface associated nucleation, the stress can be easily relieved and fewer nucleation sites are produced. Consequently, lower defect density and larger Si grains are created in FC poly-Si film. The FC TFTs with and without NH_3 plasma are shown in Fig. 6, which show a good NH_3 plasma effect. Fig. 7 shows the effective grain boundary trap density, which shows a reduced N_{trap} for the FC TFT to further verify that FC TFTs have much fewer grain boundaries trap states. Fig.8 shows the threshold voltage variation under hot-carrier stress. It is clearly observed that severe V_{TH} degradation due to easy broken of Si–Si and Si–H bonds with poor poly-Si crystallinity in CN TFTs.

4. Conclusion

We have proposed high-performance poly-Si TFTs with better crystallinity of poly-Si by a simple floating channel crystallization technique. The FC TFTs show much better performance than CN TFTs and are potentially suitable for future large-area glass applications.

Acknowledgements

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References

[1] H. Oshima and S. Morozumi, in IEDM Tech. Dig., (1989) 157.
[2] Yoshihiro Morimoto, Yushi Jinno, Kyoko Hirai, and Kiyoshi Yoneda, J. Electrochem. Soc., 144 (1997).
[3] I-W Wu, A Chiang, M Fuse, L. Ovecoglu, and T-Y Huang, J. Appl. Phys, 65 (1989) 4036.
[4] Myung-Kwan Ryu, Seok-Min Hwang, Tae-Hoon Kim, Ki-Bum Kim, and Seok-Hong Min, A. Phys. Lett., 71 (1997) 3063.
[5] Myung-Kwan Ryu, Jang-Yeon Kwon, and Ki-Bum Kim, Mat. Res. Mat. Res. Soc. Symp. Proc., 621 (2000) Q6.3.1.
[6] Tae-Hoon Kim, Myung-Kwan Ryu, and Ki-Bum Kim, Jpn. J. Appl. Phys., 37 (1998) 108.

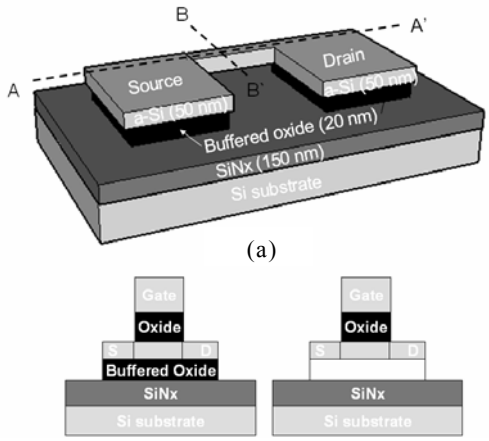

Fig. 1 (a) Bird-eye view of the FC structure. Cross-sectional view of (b) CN TFTs, and (c) FC TFTs

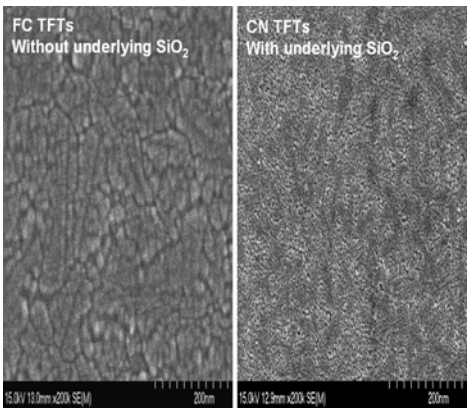

Fig. 2 SEM image of SPC poly-Si film for (a) FC structure, and (b) CN structure.

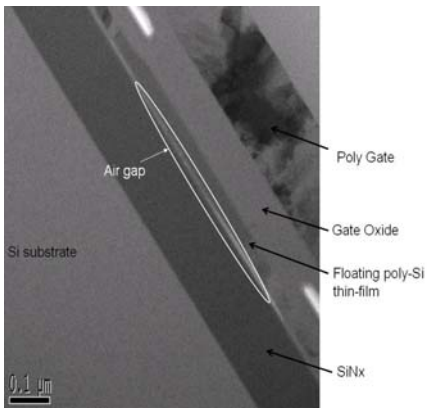

Fig. 3 Cross-sectional TEM image of the FC structure.

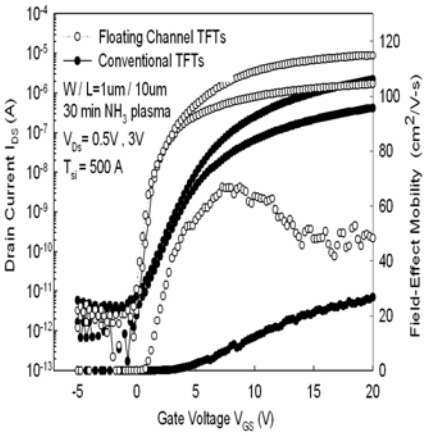

Fig. 4 Typical transfer characteristics for FC and CN TFTs (W / L =1 μm/ 10 μm).

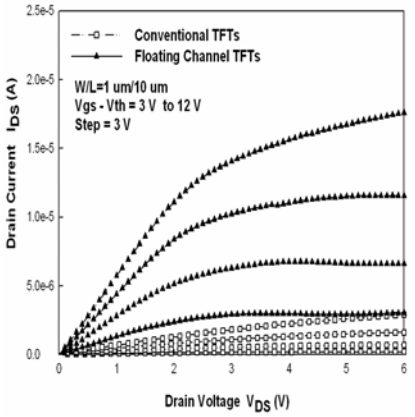

Fig. 5 Typical output characteristics for FC and CN TFTs (W / L =1 μm/ 10 μm).

Table 1 Devices characteristics comparison between FC and CN TFTs (W / L = 1 μm / 10 μm.)

Key parameters	Conventional TFTs	Floating Channel TFTs
V_{TH} (V)	6.0	1.62
S.S. (V/dec)	0.971	0.264
μ_{FE} (cm^2/V-s)	26.69	66.49
N_{Trap} (cm^{-2})	1.36×10^{12}	7.1×10^{11}
I_{ON}/I_{OFF} ratio	6.76×10^5	5.78×10^6

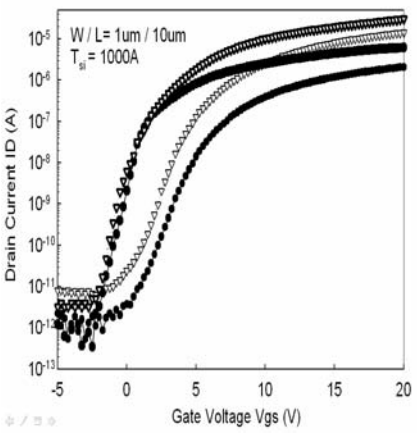

Fig. 6 Typical transfer characteristics for FC TFTs with and without NH3 plasma treatment (W / L =1 μm/ 10 μm).

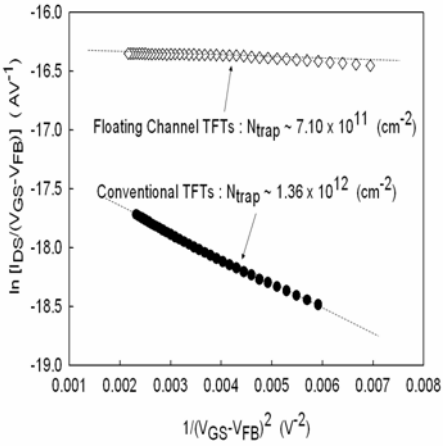

Fig. 7 Plot of ln $[I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ and the extracted effective grain-boundary trap state density for FC and CN TFTs. I_D was measured at V_D = 0.5V

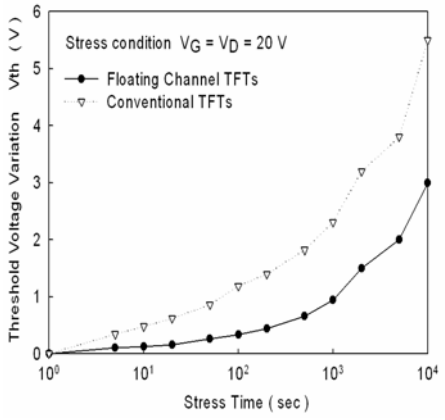

Fig. 8 Threshold voltage variation for for FC and CN TFTs (W / L =1 μm/ 10 μm).