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Low Temperature Ultra-thin Hafnium Oxide Dielectrics by Sputtering of Hf Metal on Tilted Substrate Followed by Nitric Acid Oxidation then Anodization Compensation in D. I. Water

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1. Introduction

High-quality and low-temperature dielectrics processing techniques attract much attention on fabricating poly-Si thin-film transistor (TFT) of large area displays [1]. The high-k dielectrics are considered the most promising materials for next generation TFT devices applications [2]. Among many high-k materials, hafnium oxide is of interest due to its high dielectric constant and sufficient high band-gap value [3]. Generally, a high quality SiO_2 interfacial layer can effectively minimize interface states of high-k dielectrics. However, the existing defects in the as-grown high-k dielectrics still induce bias instability problem [4].

In this study, we use a low-temperature approach of direct-current superimposed with alternating-current anodization (DAC-ANO) compensation to further repair the defects of high-k/SiO_2 stacks dielectrics. The compensation effects were verified by metal-oxide-semiconductor (MOS) structures with terraced high-k dielectrics on a single wafer. The terraced high-k dielectrics were prepared by sputtering Hf metal on tilted substrate followed by nitric acid oxidation technique. The proposed DAC-ANO compensation method is suggested a potential technique to efficiently improve the performance of low-temperature hafnium oxide dielectrics for display electronics.

2. Experiments

The MOS capacitors were prepared on the p-type (100-oriented) wafers. Then SiO_2 interlayer was initially grown by room-temperature tilted anodization process followed by rapid thermal annealing at 790^0C for 2s in N_2. The wafer was then put into the Hf sputter system at a tilted angle of about 45^0 as shown in Fig. 1(a). The as-deposited Hf film was then dipped in the nitric acid for 5 minutes in room temperature. Then the DAC-ANO compensation technique was carried out as shown in Fig. 1(b). The anodization is performed at DC=3V with alternating AC oscillation signal of 1.5V for 10 minutes. The ANO-compensated HfO_2 samples were named "HANO" and samples without compensation were named "Control" for comparison. POA was carried out in a furnace at 380^0C for 10 minutes. The pure aluminum (Al) was evaporated as the gate electrode. The gate area of 2.25×10^{-4} cm^2 was defined by UV-photolithography. Capacitance-voltage (C-V) curves were measured by an HP-4284 LCR meter and current-voltage (I-V) curves by an HP-4140B PA meter.

3. Results and Discussion

I-V characteristics of EOT=2.3nm HANO and Control samples are shown in Fig. 2. The inset of Fig. 2 shows 100 k and 1 MHz C-V curves. The gate leakage current of control is suppressed after receiving DAC-ANO compensation treatment. The statistics of EOT's distributions with +X positions in space on the wafers of HANO and control samples are revealed in Fig. 3. The illustration of the measured areas in space is shown in the inset of Fig. 3. The decrease of EOT's of HANO samples is attributed to that the dielectric constant of HANO is increased by suitably repairing the Hf-O bondings during the DAC-ANO compensation process. Fig. 4 shows the I-V characteristics of HANO samples with EOT's of 1.9, 2.1 and 2.3nm. The cumulative distributions of gate leakage currents (J_{leak}) measured at $V_G=V_{FB}$-1V for HANO are shown in Fig. 5. The J_{leak} distributions of HANO samples are uniform. The frequency dispersion distribution is shown in Fig. 6. HANO samples exhibit smaller series resistance and therefore smaller ΔC with respect to control ones. The dielectric breakdown characteristics for 15 devices of HANO samples are shown in Fig. 7. The inset of Fig. 7 shows the cumulative distributions of effective breakdown field ($E_{BD(effective)}$). $E_{BD(effective)}$ of HANO devices is over 12 MV/cm. The stress reliability of HANO and control samples is studied by performing constant current stressing (CCS) on MOS devices as shown in Fig. 8. The voltage variation of HANO after 500 seconds CCS test is smaller than control one. It is supposed that the imperfect Hf-O bondings in HfO_2 are repaired and therefore the dielectric quality is improved due to ANO compensation.

4. Conclusions

The low-temperature hafnium oxides were successfully prepared through the tilted sputter system and further compensation process. The well-behaved C-V characteristics, low leakage currents, large $E_{BD(effective)}$, and improved stress reliability indicate that the proposed DAC-ANO compensation technique is of interest for low-temperature hafnium oxides. The demonstrated low temperature technique is supposed to be useful for the applications on system-on-panel-integration, large area display system, and flexible electronics.

Acknowledgements

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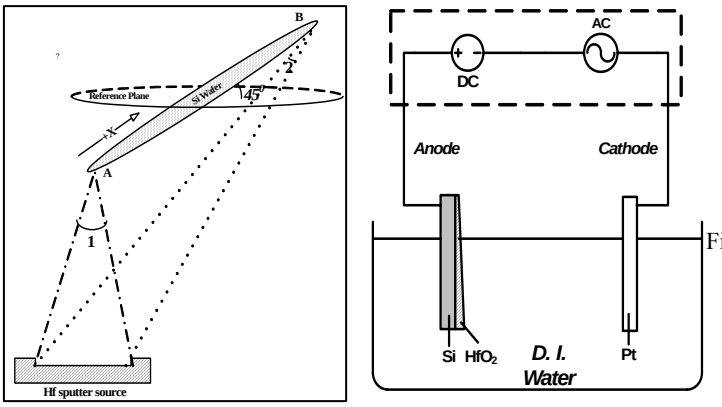

(a) (b)

Fig. 1 The illustration of (a) tilted substrate sputtering system and (b) DAC-ANO compensation system.

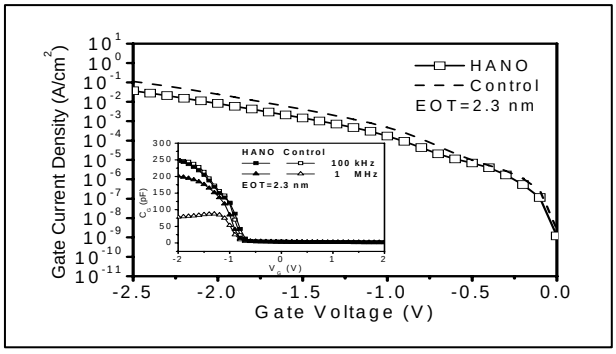

Fig. 2 Comparsion of I-V curves of HANO and control samples. The C-V characteristics are shown in the inset.

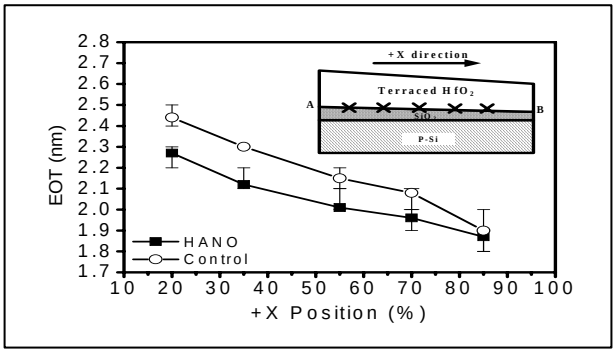

Fig. 3 The relation between EOT and x-axis position for HANO and control samples. The inset shows the terraced oxide structure and the measured areas (x).

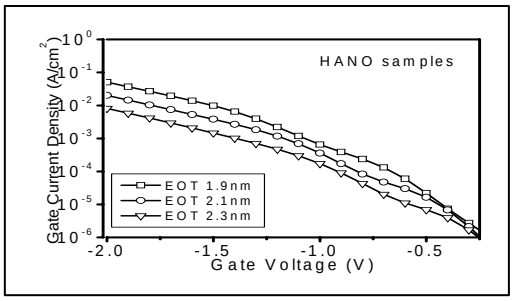

Fig. 4 I-V curves of HANO samples with EOT's=1.9, 2.1, and 2.3nm.

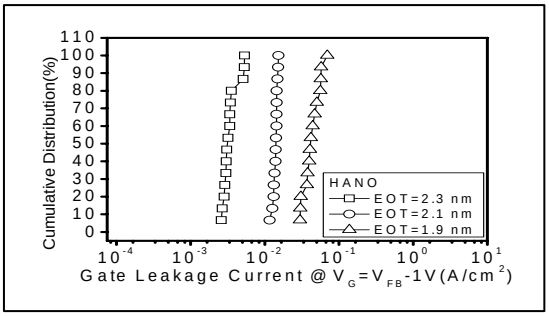

Fig. 5 The J_{leak} cumulative distribution of various HANO samples.

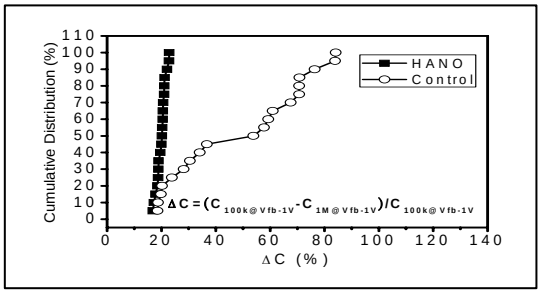

Fig. 6 Cumulative distributions of frequency dispersion for HANO and Control samples.

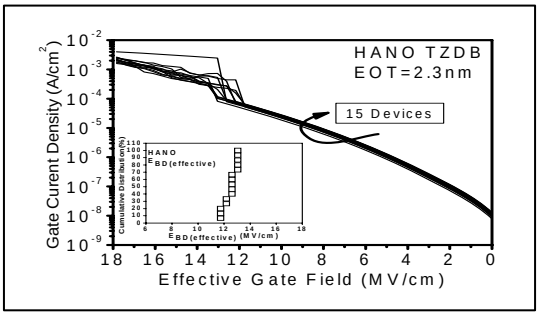

Fig. 7 TZDB characteristics of HANO samples with 15 devices. The inset shows the cumulative plot of $E_{BD(effective)}$.

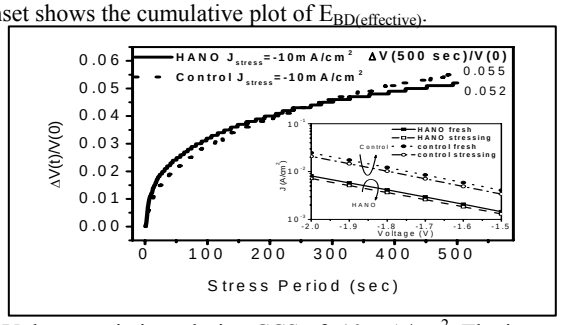

Fig. 8 Voltage variations during CCS of -10 mA/cm^2. The inset shows the J-V curves before and after stressing for HANO and control samples.