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Next Generation High-Efficiency RF Transmitter Technology for Basestations

Peter Asbeck, Don Kimball, Jinho Jeong*, Paul Draxler, Chin Hsia and Lawrence Larson

University of California, San Diego
9500 Gilman Drive, La Jolla, CA, 92093-0407 USA
Phone: +1-85-534-6713 E-mail: asbeck@ece.ucsd.edu
*Kwangwoon University, Seoul, KOREA

1. Introduction

Future wireless basestations require increasing levels of power efficiency while maintaining high signal accuracy. Increasing bandwidths to 20 MHz and beyond is also required to meet the needs for multi-carrier WCDMA transmissions and for OFDM-based systems. GaN HEMT technology is very well matched to these requirements, and is emerging as a device technology of choice for future high efficiency basestations. The amplifier architecture chosen can significantly impact the results obtained. This paper summarizes results obtained with the Envelope Tracking (ET) architecture. High efficiency (above 50%) together with high linearity is demonstrated for WCDMA signals with 7.8dB peak-to-average power ratio. Requirements for transistors in order to achieve high performance in envelope tracking are highlighted, particularly low voltage dependence of output capacitance. RF amplifier configurations to be used with ET are reviewed, including the overdriven Class J mode of operation, which can be easily achieved with GaN devices.

2. Envelope Tracking Architecture

In the envelope tracking (ET) architecture, the power supply voltage for the RF stage is varied dynamically in accordance with the signal level, in order to maintain operation at high efficiency at all times (since the output transistor operates always in compression). To implement

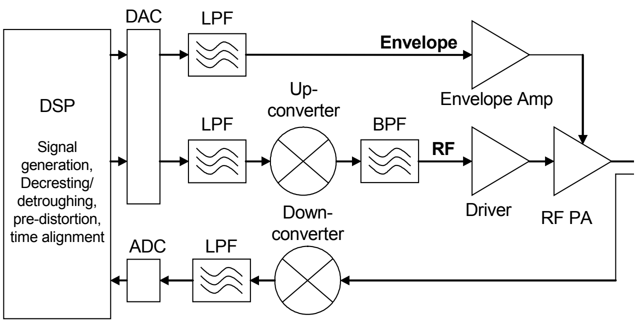

Figure 1: Block diagram of envelope tracking amplifier.

the structure, a wideband power supply with high efficiency must be employed. In our work, the design approach of figure 2 has been employed. A very high efficiency switching stage implementing a buck converter, responsible primarily for the low frequency components of the power supply output, is combined with a linear stage which has broad bandwidth and high fidelity (obtained by means of feedback), albeit with lower efficiency operation. The combined power supply can provide over 200W peak power and provides power to over 10MHz large signal bandwidth, with average efficiency ranging from 70 to 85% according to the characteristics of the signal amplified.

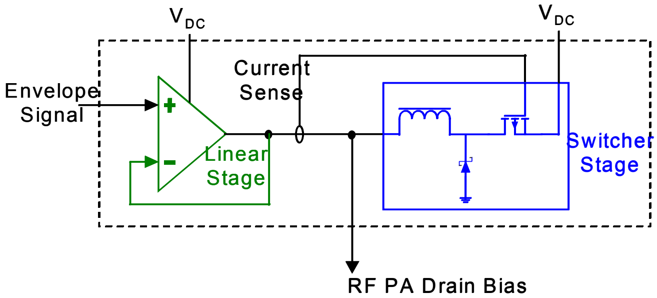

Figure 2: Schematic circuit diagram of dynamic power supply for ET applications.

To maintain linearity of the overall amplifier, an adaptive predistortion system is implemented with digital signal processing. The overall system carries out the full RF transmitter functions, including upconversion, power control and filtering.

3. ET Amplifiers with GaN HEMTs

Although ET can be applied with a variety of RF power amplifier configurations (such as Class E, Class F, Class AB), and various device technologies (GaAs HFET, Si LDMOS, GaN HEMT), we have found superior results from the use of overdriven Class J amplifiers [1] implemented with GaN devices. Using a GaN HFET fabricated on a Si substrate, overall efficiency of 50.7% was obtained for a single carrier WCDMA signal at 2.14GHz, with an associated ACLR1 value of -51dBc (and peak-to-average power ratio of 7.8dB) [2]. For these results. the dynamic power supply operated with an efficiency of 75%, while the RF stage operated with a power-added efficiency of 73%. In order to characterize the output devices, the instantaneous drain current and voltage of the output stage are recorded. Figure 3 illustrates the composite data of instantaneous PAE vs output power for the RF stage while amplifying a WCDMA signal. The instantaneous efficiency exceeds 70% over a large output power range. The efficiency is higher than has been measured on a CW basis for comparable output powers, because of the significantly reduced device heating during ET operation.
Simulations of amplifier operation indicate that high efficiency over a wide range of power supply voltages can be obtained for GaN devices operated in Class J mode.

Here the RF fundamental frequency is terminated in a load

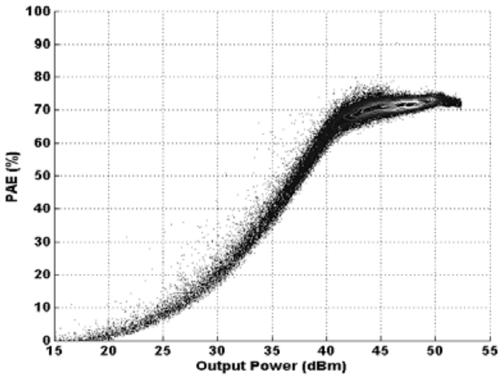

Figure 3: Measured instantaneous power-added-efficiency vs output power obtained during ET operation of a GaN HFET with a WCDMA signal.

that has inductive reactance in addition to the load resistance, and the harmonic output termination is established by the intrinsic output capacitance of the transistor. It is shown by simulation that the waveform of the current within the device *excluding the current component flowing through the device output capacitance* has a waveform exhibiting a double peak behavior, as

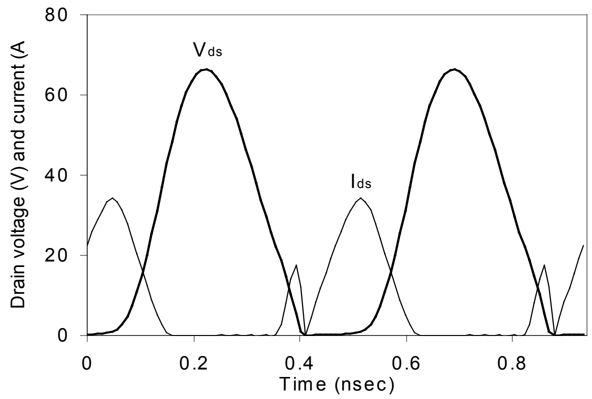

Figure 4: Simulated waveforms of drain voltage and drain current (excluding output capacitance current) for overdriven Class J operation.

shown in figure 4. The current spike coincides with the discharge of the output capacitance. A benefit of the Class J amplifier is that for low output powers (which in ET amplifiers imply low input power level and low power supply voltage) the gain does not degrade very much (in contrast to Class E).

In the amplifier measurement system, the instantaneous input amplitude and output amplitude are also recorded. A representative plot of normalized output vs input power is shown in figure 5 (for WCDMA operation). The data illustrate that the (uncorrected) input-output relationship is nonlinear, although unlike the gain saturation usually found in Class AB amplifiers, here the nonlinear region occurs at low power and low bias levels, where the gain decreases. A predistortion system is employed to linearize the operation, leading to the plot shown in figure 5b. The finite width of the line thus obtained corresponds to residual errors in the output, most of which results from "memory effects". Such effects can be caused by device traps, device self-heating, bias circuit effects and imperfect frequency response of the upconverter components, among others. The residual error

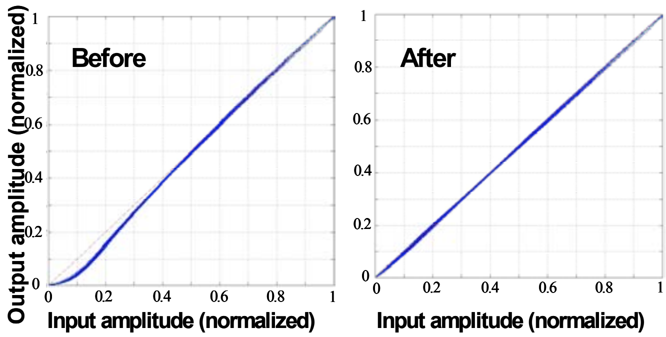

Figure 4: Measured normalized output envelope vs input envelope for GaN HFET: a) before, and b) after digital predistortion.

corresponds typically to below 5% (and below 2% after "memory effect mitigation" in DSP). It is noteworthy that the memory effect magnitude we have observed with other device technologies, such as LDMOS and GaAs HFETs,

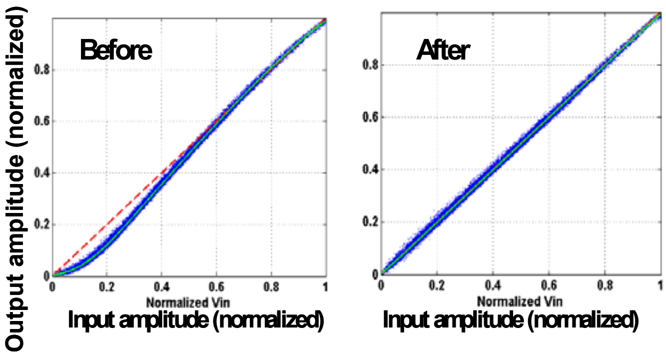

Figure 5: Normalized output envelope vs input envelope as in figure 4, measured for LDMOS-based RF stage.

has tended to be larger than that for GaN HFETs in our system. Figure 6 a and b show, for example, curves comparable to those of figure 5, measured with a Si LDMOS device.

Summary

GaN HFETs operating in envelope tracking amplifiers have been shown to offer superior efficiency, while meeting requirements of linearity, power, gain and bandwidth for next generation basestation power amplifiers.

References

[1] D. Kimball, J. Jeong, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L. Larson, and P. Asbeck, IEEE Trans. Micr. Theory and Tech., vol.54, no.11, Nov. 2006, pp. 3848-56.

[2] S. Cripps*, RF Power Amplifiers for Wireless Communications,* 2nd Ed., Artech House (2006).