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PCA-based Object Detection/Recognition Chip for Wireless Interconnected 3-D Integration

Hiroshi Ando, Seiji Kameda, Daisuke Arizono, Norimitsu Fuchigami, Kouta Kaya, Mamoru Sasaki, and Atsushi Iwata

Graduate School of Advanced Sciences of Matter, Hiroshima University
1-3-1, Kagamiyama, Higashi-Hiroshima, Hiroshima 739-8530, Japan
Phone: +81-82-422-7358 E-mail: ando@dsl.hiroshima-u.ac.jp

1. Introduction

A realization of object detection/recognition system which can recognize various objects in real-time/real-world is a very difficult and challenging subject for present computers. Such human-like system is indispensable for security, robots, ubiquitous network, etc., in a future society.

In order to integrate such a brain like system with small-size and low-power dissipation, 3-D integration of multi chips is required. Each chip has processing functions including memories, and multi-ten Gbps wideband data interfaces with low-power dissipation.

To solve the problem, we have proposed the 3-D custom stack system (3DCSS) using two kinds of wireless interconnections: inductive coupling local wireless interconnect (LWI) and antenna coupling global wireless interconnect (GWI) [1]. We have also demonstrated low power, high bit rate interconnection characteristics of them [2,3].

In this paper, we propose the object detection/recognition chip (DR3D) implementing "Eigenfaces" method based on PCA (Principal Component Analysis) [4,5] with LWI and GWI interfaces for 3DCSS.

2. PCA-based object detection/recognition algorithm

A fundamental of the Eigenfaces algorithm is explained briefly. An i-th face image is represented as a row vector $\mathbf{\Gamma}_i$. A preprocessed face $\mathbf{\Phi}_i$ is defined by $\mathbf{\Phi}_i=\mathbf{\Gamma}_i-\mathbf{\Psi}$, where $\mathbf{\Psi}$ represents the average face vector of N images including all individuals, that is $\Psi=\sum_{n=1}^{N}\Gamma_n \big/ N$. The "eigenfaces" can be calculated as the eigenvectors $\mathbf{a}_k$ (in an ascending order, k=1, 2, $\cdots$, m) of the covariance matrix $\boldsymbol{C}$ of N images, $C=\sum_{n=1}^{M}\Phi_n\Phi_n^t \big/ M$, where $\mathbf{\Phi}^t$ is a transposed matrix and M is the number of pixels. By using these eigenvectors, we can project an input face image into eigenspace by a simple equation: $\omega_k=\mathbf{a}_k^t\mathbf{\Phi}_i$.

Face detection is performed by generally used thresholding methods. A reconstructed image $\mathbf{\Phi}_r$ defined by $\Phi_r=\sum_{k=1}^{m}\omega_k\mathbf{a}_k$ is used as an input of evaluation function for thresholding. An unknown input image is classified as a face when the Euclidean distance $\varepsilon=\|\mathbf{\Phi}_{in}-\mathbf{\Phi}_r\|$ is lower than a threshold, where $\mathbf{\Phi}_{in}$ is a preprocessed unknown input image.

Face recognition is performed with similar calculations except for needing individual's average face vector and eigenvectors calculated by using only individual's images. An unknown input face image is classified as a j-th individual when $\varepsilon_j=\|\mathbf{\Phi}_{in}-\mathbf{\Phi}_{j,r}\|$, where $\mathbf{\Phi}_{j,r}$ is a j-th individual's reconstructed image, is the smallest value for all individuals.

3. Hardware implementation

Multi-object recognition system

A schematic of the proposed multi-object recognition system is shown in Fig. 1. This system consists of three kinds of chips, that is Visual Processing chip (VP3D), Detection/Recognition chip (DR3D) and Reference Memory chip (RM3D). Each chip has multi-channel LWIs which can transmit to and receive data from neighboring chips simultaneously and 2ch GWIs for clock and reference data receiving. The RM3D has 2ch GWIs and transmitter circuits for clock and reference data.

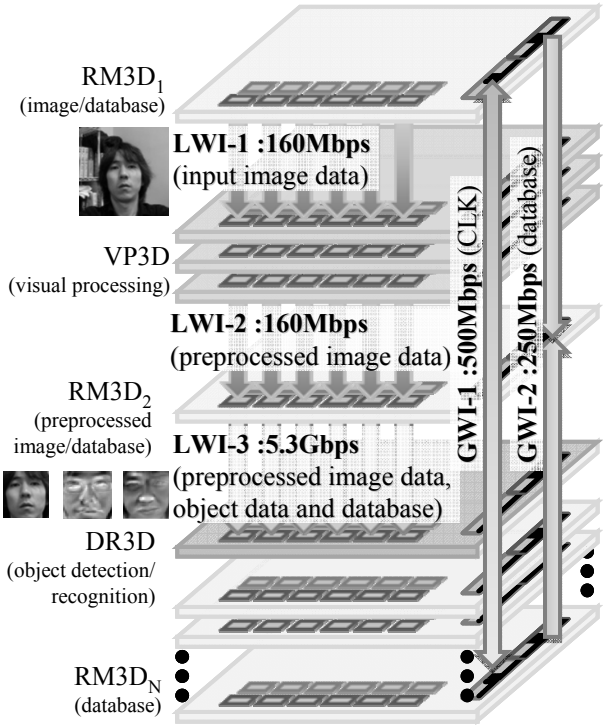

Fig. 1 Multi-object recognition system. The transfer rates are derived from 250MHz clock frequency and 21-channel LWIs.

The operation of this system is as follows. At first, original image data supplied by wire interface is stored in $RM3D_1$ and transferred to neighboring VP3D by LWI-1 with PWM (pulse width modulation) signaling. Second, parallel image pre-processing for noise suppression and

feature enhancements are implemented by several VP3Ds and resulted image data are transferred to $RM3D_2$ with LWI-2. Finally, the processed image data and object database are transferred to DR3D through LWI-3 with bit rate of 5.3Gbps and detects and recognizes objects. Although the memory capacity of $RM3D_2$ is limited, recognition of further objects can be implemented by transferring reference data from $RM3D_N$ to $RM3D_2$ by GWI-2.

Object detection/recognition circuits - DR3D design

A block diagram of the DR3D is shown in Fig. 2. The DR3D was designed to execute two functions of object detection and recognition with common use of the same circuit blocks. This advantage is provided by utilizing the Eigenfaces algorithm. The pixel sizes of an input image and an object are 84x84 and 32x32, respectively.

At first, 21bit digital input data for one pixel (8bit raw image vector: $\mathbf{\Gamma}$, 8bit average face vector: $\mathbf{\Psi}$ and 5bit eigenvector: $\mathbf{a}$) are transferred from RM3D to each 32x32 shift registers through the 21-channel parallel LWIs. These data are converted to 32-pixel parallel data by shift-register. Second, reconstructed image data $\mathbf{\Phi}_i=\mathbf{\Gamma}_i-\mathbf{\Psi}$ are calculated by subtracter, $\omega_k=\mathbf{a}_k{}^t\mathbf{\Phi}_i$ are calculated by multipliers and $\Phi_r=\sum_{k=1}^{m}\omega_k\mathbf{a}_k$ are obtained by accumulators. Finally, Manhattan distance $\varepsilon=\|\mathbf{\Phi}_{in}-\mathbf{\Phi}_r\|$ and $\varepsilon_j=\|\mathbf{\Phi}_{in}-\mathbf{\Phi}_{j,r}\|$ are calculated with subtracter and compared in Winner-take-all circuits, detection or recognition process is finished.

The global system clock signal is transferred from the RM3D chip with system control function by GWI.

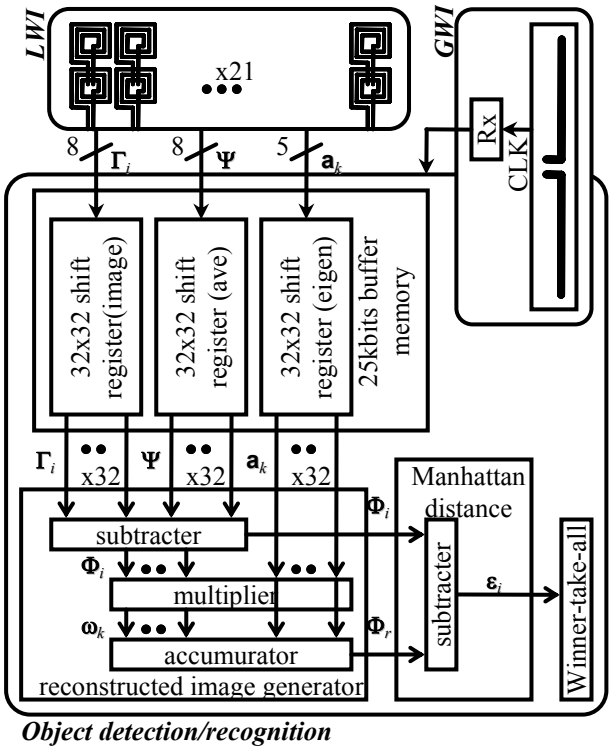

Fig. 2 Block diagram of DR3D.

Fabrication and integration

Test chip of DR3D fabricated with a 0.18μm CMOS technology is shown in Fig. 3. The chip size is 5mm x 5mm, the supply voltage is 1.8V. The operation frequency is 250MHz, the data transfer rates of LWI and GWI are 250Mbps/ch and 500Mbps/ch, respectively. The power dissipation of the LWI is 1.6mW/ch @ 250MHz. The GWI power dissipation is 56mW. Processing capability of 40GOPS was realized with the total LWI data bandwidth of 5.3Gbps.

Although the system performance is not measured, detection time and one-to-one (one detected object to one object of database) recognition time are estimated to be 580μs and 4.2μs by the simulation, respectively.

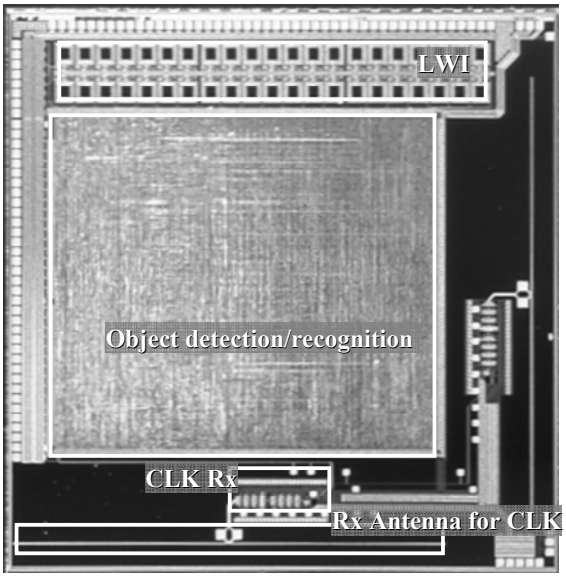

Fig. 3 Microphotograph of DR3D.

4. Conclusions

The object detection/recognition chip was designed by utilizing the algorithm based on Eigenfaces method and the 3-D integration scheme with LWI and GWI. Wideband wireless chip-to-chip interconnections of 5.3Gbps parallel LWI for image data and 500Mbps GWI for clock were utilized. By the performance prospect of fabricated chip with a 0.18μm CMOS technology, object detection/recognition system performance of 580μs detection, 4.2μs one-to-one recognition, and 40GOPS processing capabilities at 250MHz were estimated.

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