An unknown input face image is classified as an eigenvector calculated using only individual’s images. For this purpose, we need individual’s average face vector and face when the Euclidean distance for thresholding. An unknown input image is classified as an individual when \( \varepsilon = ||\Phi_{i} - \Phi_{j}|| \), where \( \Phi_{j} \) is a \( j \)-th individual’s reconstructed image, is the smallest value for all individuals.

3. Hardware implementation

Multi-object recognition system

A schematic of the proposed multi-object recognition system is shown in Fig. 1. This system consists of three kinds of chips, that is Visual Processing chip (VP3D), Detection/Recognition chip (DR3D) and Reference Memory chip (RM3D). Each chip has multi-channel LWIs which can transmit to and receive data from neighboring chips simultaneously and 2ch GWIs for clock and reference data receiving. The RM3D has 2ch GWIs and transmitter circuits for clock and reference data.

![Fig. 1 Multi-object recognition system. The transfer rates are derived from 250MHz clock frequency and 21-channel LWIs.](image-url)
feature enhancements are implemented by several VP3Ds and resulted image data are transferred to RM3D₂ with LWI-2. Finally, the processed image data and object database are transferred to DR3D through LWI-3 with bit rate of 5.3Gbps and detects and recognizes objects. Although the memory capacity of RM3D₂ is limited, recognition of further objects can be implemented by transferring reference data from RM3Dₙ to RM3D₂ by GWI-2.

Object detection/recognition circuits - DR3D design

A block diagram of the DR3D is shown in Fig. 2. The DR3D was designed to execute two functions of object detection and recognition with common use of the same circuit blocks. This advantage is provided by utilizing the Eigenfaces algorithm. The pixel sizes of an input image and an object are 84x84 and 32x32, respectively.

At first, 21bit digital input data for one pixel (8bit raw image vector: \( \Gamma \), 8bit average face vector: \( \Psi \) and 5bit eigenvector: \( a \)) are transferred from RM3D to each 32x32 shift registers through the 21-channel parallel LWIs. These data are converted to 32-pixel parallel data by shift-register. Second, reconstructed image data \( \Phi_i = \Gamma_i - \Psi \) are calculated by subtracter, \( \omega_k = a_k \) are calculated by multipliers and \( \Phi_r = \sum_k \omega_k a_k \) are obtained by accumulators. Finally, Manhattan distance \( \varepsilon = | \Phi_m - \Phi_r | \) and \( \varepsilon = | \Phi_m - \Phi_d | \) are calculated with subtracter and compared in Winner-take-all circuits, detection or recognition process is finished.

The global system clock signal is transferred from the RM3D chip with system control function by GWI.

Fabrication and integration

Test chip of DR3D fabricated with a 0.18µm CMOS technology is shown in Fig. 3. The chip size is 5mm x 5mm, the supply voltage is 1.8V. The operation frequency is 250MHz, the data transfer rates of LWI and GWI are 250Mbps/ch and 500Mbps/ch, respectively. The power dissipation of the LWI is 1.6mW/ch @ 250MHz. The GWI power dissipation is 56mW. Processing capability of 40GOPS was realized with the total LWI data bandwidth of 5.3Gbps.

Although the system performance is not measured, detection time and one-to-one (one detected object to one object of database) recognition time are estimated to be 580µs and 4.2µs by the simulation, respectively.

4. Conclusions

The object detection/recognition chip was designed by utilizing the algorithm based on Eigenfaces method and the 3-D integration scheme with LWI and GWI. Wideband wireless chip-to-chip interconnections of 5.3Gbps parallel LWI for image data and 500Mbps GWI for clock were utilized. By the performance prospect of fabricated chip with a 0.18µm CMOS technology, object detection/recognition system performance of 580µs detection, 4.2µs one-to-one recognition, and 40GOPS processing capabilities at 250MHz were estimated.

References