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Capacitor-Shunted Transmitter for Power Reduction in Inductive-Coupling Clock Link

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1. Introduction

Recently there has been a lot of interest in the field of wireless chip to chip communication. Several papers [1-2] have reported high bandwidth for data transmission which also use wireless clock recovery circuits. The clock link in this scheme consumes more power than the data link [1]. The conventional wireless clock link uses H-Bridge transmitter to transmit the clock. This paper presents a simple and novel circuit namely Capacitor-shunted transmitter. A test chip is fabricated in 0.18μm Technology and the measurement shows that the power consumption of the transmitter is reduced by about 50%.

Figure 1 presents the conceptual diagram of the inductively coupled clock transceiver. Clock of the transmitter *Txclk* is transmitted from the upper metallic inductor which produces a magnetic field and the change in this magnetic field produces an induced voltage at the receiver inductor. The receiver senses the voltage and clock of the receiver *Rxclk* is recovered by the clock transceiver. The clock frequency is varied from 0.65GHz to 1.6GHz to check the power dissipation for varying frequency.

2. Capacitor-Shunted Transmitter

Figure 2(a) presents the schematic diagram and the simulation result of the conventional H-Bridge transmitter. Figure 2(b) present the schematic diagram and the simulation result of the proposed Capacitor-shunted transmitter. The transmitter transmits the clock *Txclk* which produces the current I_{TC} at the transmitter inductor. This change in current produces an induced voltage V_{RC} at the receiver inductor. The receiver recovers the clock *Rxclk* as shown in the figure. The power consumed P_{TX} as a function of time is also shown to compare between the H-Bridge and the Capacitor-shunted transmitter.

The capacitor shunted transmitter consumes power only during the charging time of the capacitor; hence the power consumed is reduced to half. A hysterisis comparator is used as a receiver.

3. Test Chip Measurement

Figure 3 shows microphotograph of the test chips fabricated in 0.18μm CMOS. The receiver chip is placed on top of the transmitter chip, for both the chips to be in face up position. The upper chip is polished to 10μm thickness. Communication distance including an adhesive layer is 15μm. The clock transceiver transmits 1GHz clock by the metal inductor with a diameter of 200μm. Two transmitter circuits are investigated namely the H-Bridge and the Capacitor-shunted transmitter circuit.

Figure 4 shows the received clock at the receiver along with the schematic of the experimental setup. RMS jitter is 1.6ps in *Rxclk*, some of which is caused by 1ps jitter in *Txclk* by an external clock generator at 1GHz.

Figure 5 shows the power dissipation as a function of frequency for both the H-Bridge transmitter and also the Capacitor-shunted transmitter. The H-Bridge clock transmitter consumes 1.5mW of power whereas the Capacitor-shunted transmitter consumes 0.75mW of power at 1GHz.

4. Conclusion

A novel Capacitor-shunted clock-link transceiver was investigated. A test chip was fabricated in TSMC 0.18μm CMOS. Simulation results and the measurement results show that the new Capacitor-shunted transmitter consumes half the amount of power as compared with the H-Bridge transmitter. The performance summary of the chip is given in figure 6.

Acknowledgements

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References

[1] N. Miura, *et al*.,"A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link" *IEEE ISSCC Dig Tech. Papers*, pp.424-425, Feb. 2006.

[2] N. Miura, *et al*.,"A 0.14pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse Shaping," *ISSCC Dig. Tech. Papers*, pp.358-359, Feb. 2007.

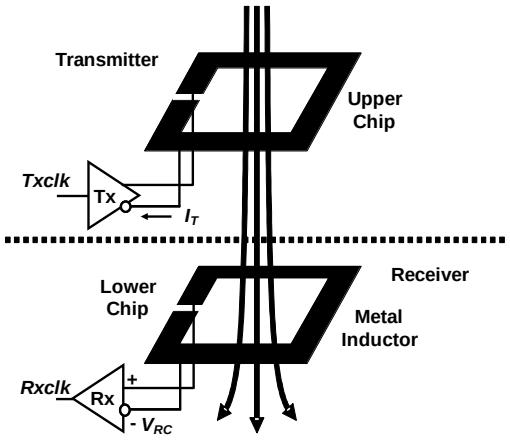

Fig.1 Inductive-coupling clock link.

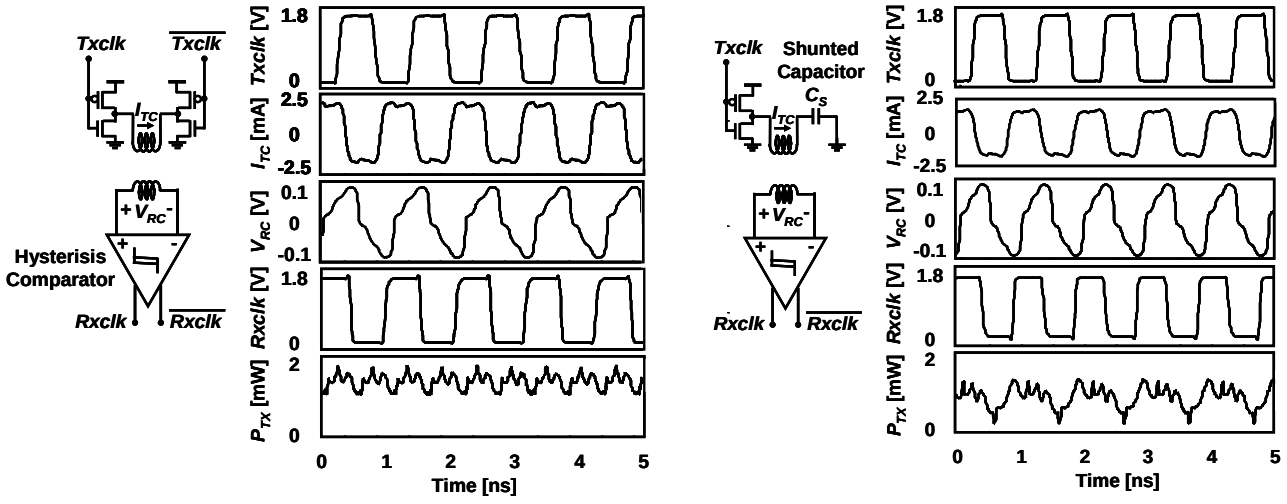

Fig.2 Schematic Diagram and Simulated waveforms for (a) H-Bridge Transmitter and (b) Capacitor-shunted Transmitter

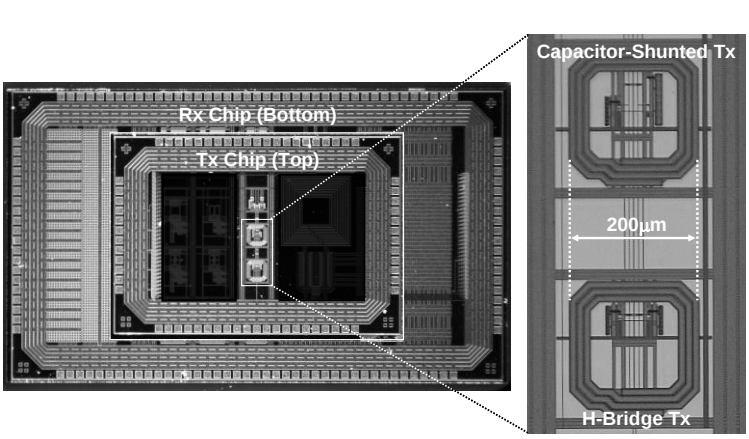

Fig.3 Microphotograph of stacked test chips.

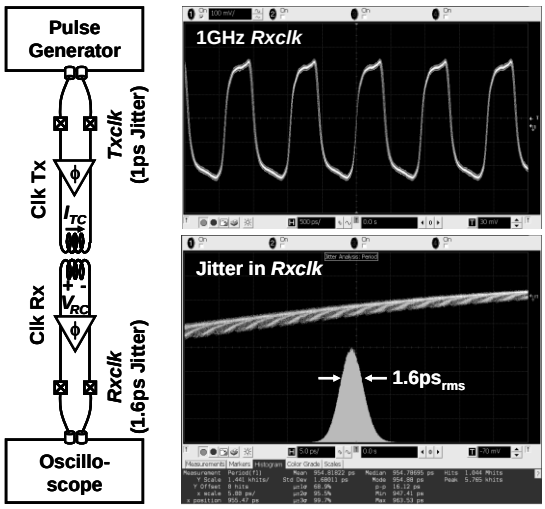

Fig.4 Measured received clock and jitter.

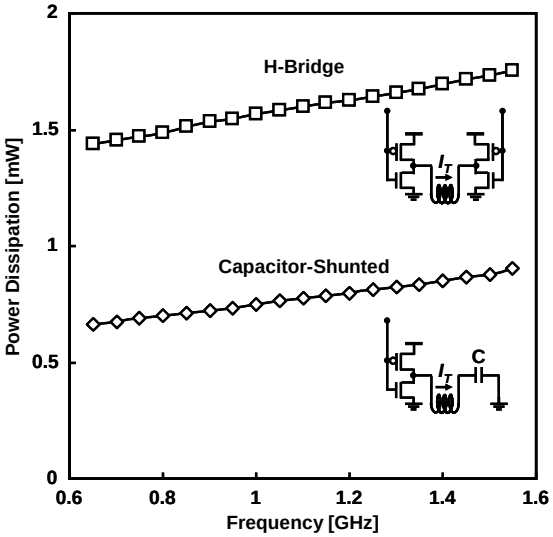

Fig.5 Measured power dissipation.

	H-Bridge Transmitter	Capacitor-Shunted Transmitter
Power Dissipation	1.55mW	0.75mW
Clock Rate	1GHz	
Channel Area	200μm x 200μm	
Distance	15μm	
Jitter	1.46ps	1.68ps
Process	180nm CMOS (V_{DD}=1.8V)	

Fig.6 Performance Summary.