Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 1070-1071

G-10-3

Scaling Characteristics of Si On-chip Integrated Antennas

K. Kimoto, N. Sasaki and T. Kikkawa

Research Center for Nanodevices and Systems, Hiroshima University
Phone: +81-082-424-6265, Fax: +81-082-424-3499
E-mail: {kimoto, kikkawa}@sxsys.hiroshima-u.ac.jp

1. Introduction

Wireless interconnect system using Si integrated antennas has been developed as an advanced intra/inter-chip signal transmission for 3-D integrated packaging of ULSI chips [1-5]. The conceptual diagram is shown in Fig. 1. Signal transmits from transmitting antennas (T_X) to receiving antennas (R_X) through stacked Si chips by utilizing electromagnetic wave.

In this paper, we present scaling characteristics for Si on-chip integrated antennas.

2. Si integrated antenna and equivalent circuit

Figures 2(a) and 2(b) show a schematic diagram of Si integrated linear dipole antennas and its equivalent circuit model which is consisted of antenna and substrate. A part of antenna was consisted of series circuit of radiation (R_{rad}), loss (R_{loss}) resistances, inductance (L_{ant}), and capacitance (C_{ant}). On the other hand, substrate is consisted of parasitic components including capacitances and resistance (C_{SiO2}, C_{Si}, R_{Si}, and $C_{Low\text{-}k}$), which are inserted between antenna and ground, because integrated antenna was fabricated on Si substrate.

Radiation efficiency (e_{rad}) was calculated by 3-D EM-filed simulator (MW-Studio, CST). Then, a radiation resistance was calculated, which was defined as $R_{rad} = \mathrm{Re}(Z_{in}) \times e_{rad}$, where $\mathrm{Re}(Z_{in})$ means real part of antenna input impedance.

3. Results and Discussion

Figure 3 shows a scaling of antenna size and ultra wideband (UWB) center frequency which is defined as one tenth of cut-off frequency (f_T) as a function of CMOS technology node. By scaling the technology node from 180 to 45 nm, the antenna length can be reduced from 7 to 2.3 mm.

Figure 4 shows influence of antenna length on radiation efficiency and antenna gain. Radiation efficiency was 13% for 5 mm-long dipole antenna. Most of power radiated from the integrated antenna fabricated on Si was absorbed into Si substrate due to difference of dielectric constants between air and Si (ε_r=12). Radiation efficiency increased with decreasing antenna length, while the antenna gain decreased. According to Friis transmission equation, antenna gain is expressed as eq. (1),

$$\frac{P_{rec}}{P_{tran}} = \left(\frac{\lambda}{4\pi R}\right)^2 G_{0tran} G_{0rec} \qquad (1)$$

,where P_{rec} and P_{tran} are receiving and transmitting power, respectively. λ and R are wavelength and distance between antennas. G_{0tran} and G_{0rec} are gain of transmitting and receiving antennas, respectively. The attenuation constant in Si substrate which defined as eq. (2),

$$\alpha = \omega\sqrt{\frac{\mu\varepsilon}{2}}\left[\sqrt{1+\left(\frac{\sigma}{\omega\varepsilon}\right)^2}-1\right]^{1/2} \qquad (2)$$

Therefore, antenna gain decreased with reducing antenna length.

Figure 5 shows influence of antenna length on radiation and loss resistances. Loss resistance decreased with decreasing antenna length. Operation frequency increased with decreasing antenna length, so that the effect of skin depth becomes more dominant and loss resistance increases. Skin depth was 0.58 μm at 20 GHz.

Figure 6 shows received peak-to-peak voltage versus antenna length. Received peak-to-peak voltage decreased with decreasing antenna length. On the other hand, antenna width did not affect radiation efficiency as shown in Fig. 7.

Figure 8 shows dependence of antenna transmission gain on thickness of Si chips at 15 GHz. Transmission gain through Si chips was measured and simulated [5]. Thickness of Si chip is 260 μm. Simulation results matched well with measurement data. Antenna gain decreased with a slope of -4.5 dB/mm due to attenuation loss in Si chip.

Table 1 shows a scaling of on-chip integrated antennas for constant transmission distance. Antenna length reduced with 1/k when transistor size scaled down with 1/k, because cut-off frequency (f_T) of transistor increased with k. Radiation resistance, loss resistance, radiation power, and radiation efficiency were calculated in the case of infinitesimal dipole antenna. Radiation efficiency decreased with $[1/(1+k^{1/2})]$ and received peak-to-peak voltage decreased with (1/k). Transmission distance decreased with $1/k(1+k^{1/2})$ for constant antenna gain. Energy per bit which is defined as V^2/Zf_c decreased with $1/k^3$, where V and Z mean supply voltage and input impedance of antenna, respectively.

4. Conclusion

Scaling characteristics of on-chip integrated antennas were investigated. As the transistor size is scaled down with 1/k, Si on-chip integrated antennas by use of electromagnetic wave transmission between chips can be scaled down in accordance with transistor scaling. The transistor size is scaled down with 1/k according to the scaling rule, the antenna length can be reduced with 1/k, and energy per bit decreases with $1/k^3$.

Acknowledgements

This work is supported by semiconductor technology academic research center (STARC).

References

[1] A. Iwata et al., IEEE Int. Solid-State Circuits Conf., 2005, p. 262.
[2] A.B.M. H. Rashid et al., IEEE Electron Devices Lett. **23** (2002) 731.
[3] A. B. M. H. Rashid et al., Jpn. J. Appl. Phys. **43** (2004) 2283.
[4] S. Watanabe et al., Jpn. J. Appl. Phys. **43** (2004) 2297.
[5] K. Kimoto et al., Jpn. J. Appl. Phys. **44**, (2005), 2761.
[6] P. K. Saha et al., Jpn. J. Appl. Phys. **45**, (2006), 3279.

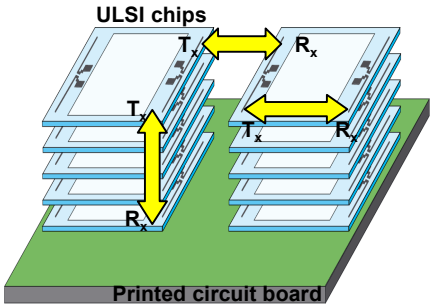

Fig. 1. Conceptual diagram of wireless interconnect system for ULSI chips using Si integrated antennas.

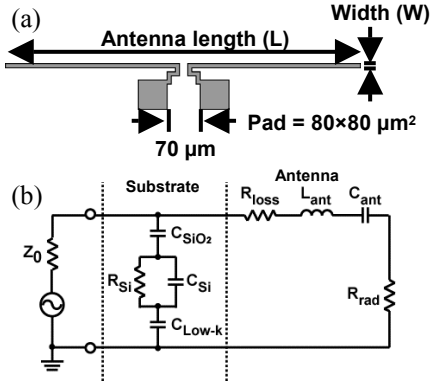

Fig. 2. On-chip integrated linear dipole antenna. (a) Schematic diagram. (b) Equivalent circuit.

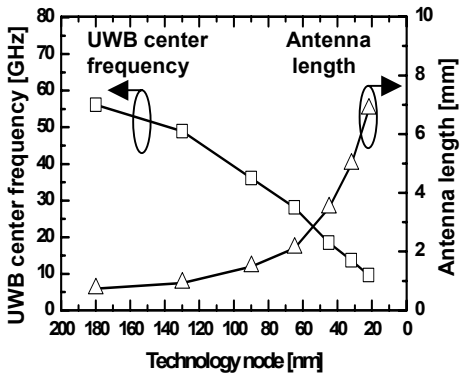

Fig. 3. Scaling of antenna size and UWB center frequency as a function of CMOS technology node.

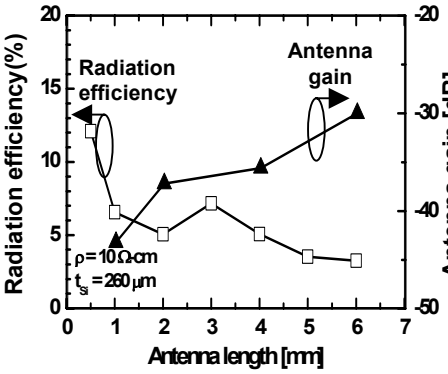

Fig. 4. Influence of antenna length on radiation efficiency and antenna gain (t_{Si}= 260 μm and ρ=10 Ω·cm).

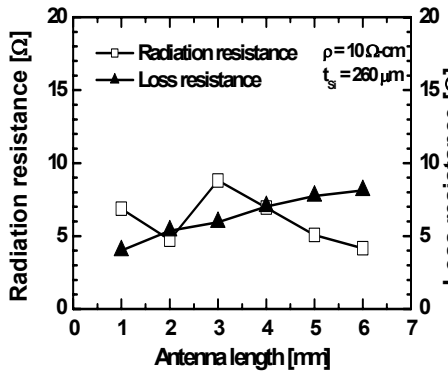

Fig. 5. Radiation and loss resistances versus antenna length (t_{Si}= 260 μm and ρ=10 Ω·cm).

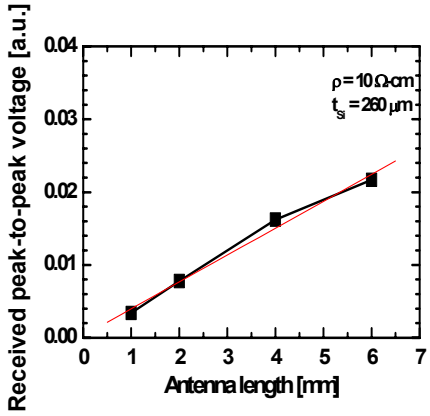

Fig. 6. Received peak-to-peak voltage versus antenna length (t_{Si}= 260 μm and ρ=10 Ω·cm).

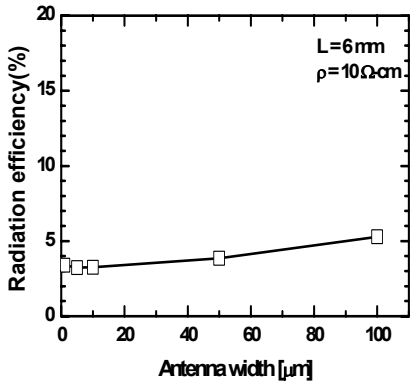

Fig. 7. Influence of antenna width on radiation efficiency (t_{Si}= 260 μm and ρ=10 Ω·cm).

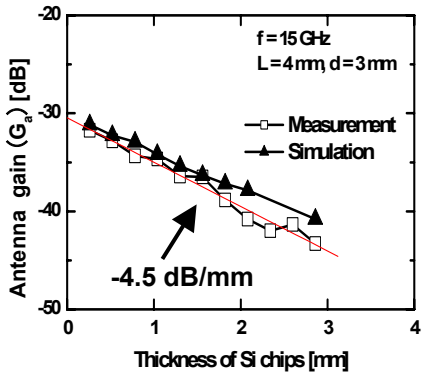

Fig. 8. Antenna transmission gain versus thickness of Si chips (L=4 mm).

Table. 1. Scaling rule of on-chip integrated antennas

Transistor size		**1/k**
Supply voltage (*V*)		**1/k**
Cut-off frequency (f_T)		**k**
Maximum frequency (f_{max})		**k**
UWB center frequency (f_c=f_T/10)		**k**
Data rate		**k**
Electromagnetic field		**1**
Antenna length (L=1/f_c)		**1/k**
Antenna current (I_0)		**1/k**
Radiation resistance	$R_{rad} = 80\pi^2 (l/\lambda)^2$	**1**
Loss resistance	$R_{loss} = l/\pi a \cdot \sqrt{2\omega\mu_0/\sigma}$	**$k^{1/2}$**
Radiation power	$P_{rad} = 40\pi^2 \lvert I_0 \rvert^2 (l/\lambda)^2$	**$1/k^2$**
Radiation efficiency	$e_{rad} = R_{rad}/(R_{rad} + R_{loss})$	**$1/(1+k^{1/2})$**
Antenna gain	$P_{rec}/P_{tran} = (\lambda/4\pi R)^2 G_{0tran} G_{0rec}$	**1**
Transmission distance		**$1/k(1+k^{1/2})$**
Received voltage (V_{pp})		**1/k**
Energy per bit (V^2/Zf_c)		**$1/k^3$**