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A Fully Integrated SiGe Optical Receiver Using Differential Active Miller Capacitor for 4.25 Gb/s Fiber Channel Application

Ji-Chen Huang, Kuang-Sheng Lai and Klaus Y.-J.Hsu

Institute of Electronics Engineering, National Tsing Hua University,
101, Section 2, Kuang Fu Road, Hsinchu, Taiwan, 30055, ROC
Phone: 886-3-5742594 Fax: 886-3-5715971 E-mail: yjhsu@ee.nthu.edu.tw

1. Introduction

Optical receivers in the transceiver modules are the key components that influence the performance and cost of optical communication networks. Conventional optical receiver is composed of a transimpedance amplifier (TIA) and a limiting amplifier (LA) in separate packages, and bond wires. The imperfections of package pins and bond wires risk the bandwidth and intersymbol interference (ISI) performance [1]. Furthermore, both the auto threshold control (ATC) circuit and dc offset cancellation (DOC) circuit need large off-chip capacitors, which degrades the reliability and raises cost. Integrating these chips in a single chip can avoid these issues.

This paper presents a 4.25 Gb/s fully integrated optical receiver that was realized in a commercial 0.35um SiGe BiCMOS process. The optical receiver incorporates a TIA, an ATC circuit, an LA, a DOC circuit, and an output stage in a single chip. In contrast to conventional receivers, our design is a single chip and does not need any separate packages and external capacitors. On-chip differential active Miller capacitor (DAMC) circuit was used to replace the conventional large off-chip capacitors.

2. Optical Receiver Architecture And DAMC Circuit

Fig. 1 shows the block diagram of the optical receiver which integrates a TIA, an ATC circuit, an LA, a DOC circuit, DAMC circuits, and an output stage in a single chip. The two-stage TIA converts the signal from single ended to pseudo-differential ended. It is designed to be with high gain and moderate bandwidth to reduce the input referred noise voltage of subsequent stages. The ATC circuit consists of a low pass filter (LPF) to convert the pseudo-differential signal to truly-differential ended. Two 0.22 nF equivalent capacitors (C_{M1}) are needed in this circuit block. The LA consists of a chain of three gain cells and amplifies the voltage swing to a logic level for data recovery. The DOC circuit consists a LPF to eliminate the dc offset voltage. It needs two 1.43 nF equivalent capacitors (C_{M2}).

In this design, the whole circuit blocks are directly coupled on the chip to avoid off-chip noise interference. Because the TIA and LA are fully integrated on a single chip, it becomes difficult to measure and characterize their frequency response separately. The simulated frequency response is shown in Fig. 2. The conversion gain and the $f_{H\text{-}3dB}$ of the TIA, the LA, and the optical receiver are (66 dBΩ, 2.9 GHz), (60dB, 3.3GHz), and (126 dBΩ, 2.55GHz), respectively. The $f_{L\text{-}3dB}$ of the LA and the optical receiver is 35 KHz. Because of the low $f_{L\text{-}3dB}$ value, the optical receiver needs large equivalent capacitors C_{M1} and C_{M2}. Fig. 3 illustrates a new DAMC circuit that realizes the large equivalent capacitors. The real capacitors (C_{MA}) are amplified by the differential amplifier due to the Miller effect [2]. The values of the real capacitors (C_{MA}) in the ATC circuit and DOC circuit are only 13.7 pF and 44.8 pF, respectively, which leads to enormous savings of chip area. The design methodology can achieve both low-cost and high reliability design.

3. Measurement Results

In the measurement, 2^{31}-1 pseudorandom bit sequence pattern was used. Fig. 4 indicates that the DAMC circuits in the ATC circuit and the DOC circuit are functional because the two output terminal results as measured in panel 3 and panel 4 have very precise crossing points (crossing percentage equals 50.1%) and minimal dc offset. The eye diagrams were defined at a bit-error rate (BER) of 10^{-12} using the 2^{31}-1 pseudorandom bit sequence pattern for a current level of 2000 $\mu A_{p\text{-}p}$. The data jitter and the differential output swing are 44.84 ps and 508 $mV_{p\text{-}p}$, respectively. Fig. 5 shows that the BER is less than 10^{-12} over an input current dynamic range from 600 $\mu A_{p\text{-}p}$ to 4100 $\mu A_{p\text{-}p}$ (16.7 dB). Under 3.3 V supply, the power dissipation of the receiver is 105.6 mW. Fig. 6 shows that the chip size of the optical receiver is 940 μm x 985 μm.

4. Conclusions

This paper presents the implementation of a fully integrated SiGe 4.25 Gb/s optical receiver without any off-chip devices. The design uses a new high performance differential active Miller capacitor (DAMC) circuit to eliminate the need of using external capacitors. Our proposed single-chip optical receiver is suitable for high performance, low-cost and high-speed optical communication applications.

Acknowledgements

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References

[1] B. Razavi, *Design of integrated circuits for optical communications*, 2003, p. 18.

[2] P. R. Gray et al., *Analysis and design of analog integrated circuits*, 2001, p. 488.

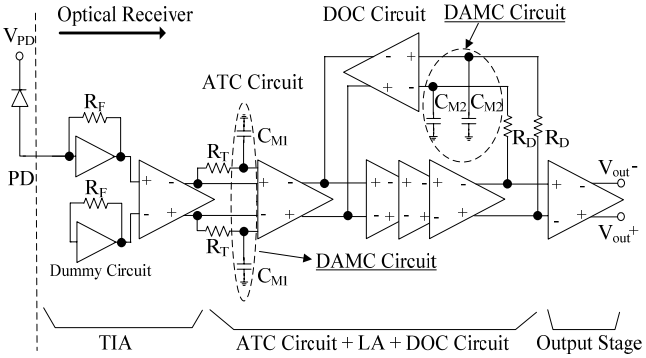

Fig. 1 The optical receiver architecture.

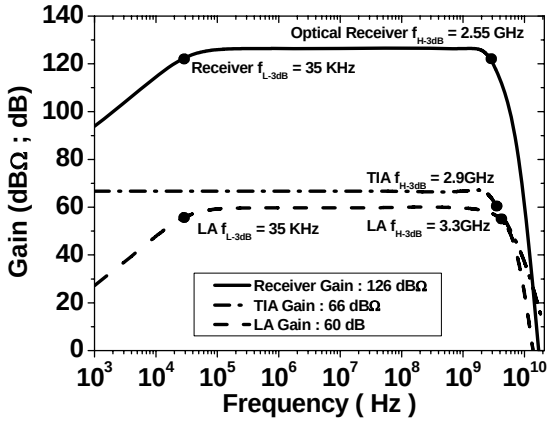

Fig. 2 Simulated frequency response of the circuits in the optical receiver.

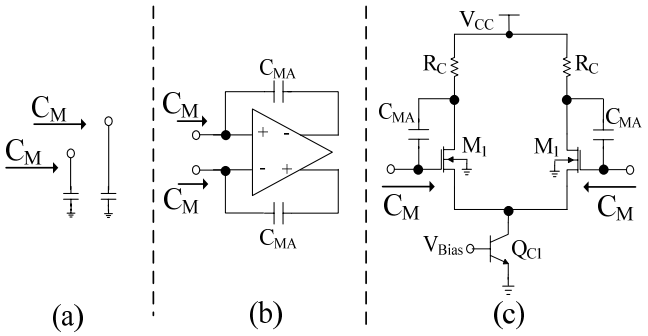

Fig. 3 (a) The capacitor circuit schematic. (b) The DAMC equivalent model. (c) The DAMC schematic.

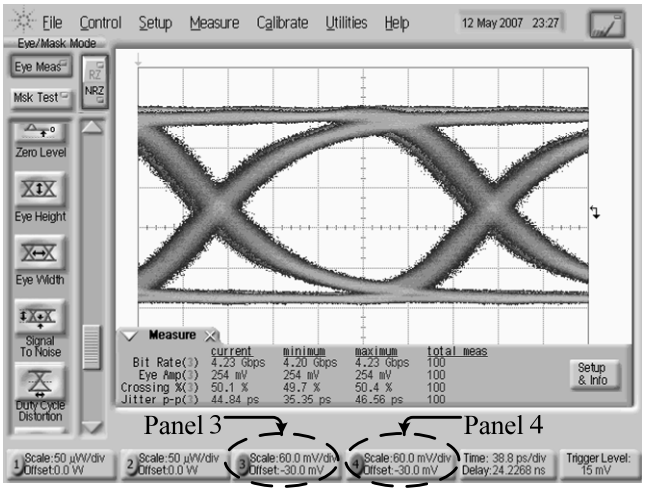

Fig. 4 The eye diagrams of the two output terminals with 2000 μA_{p-p} input using 2^{31}-1 PRBS at BER = 10^{-12}. Y-scale: 60 mV/div, x-scale: 38.8 ps/div.

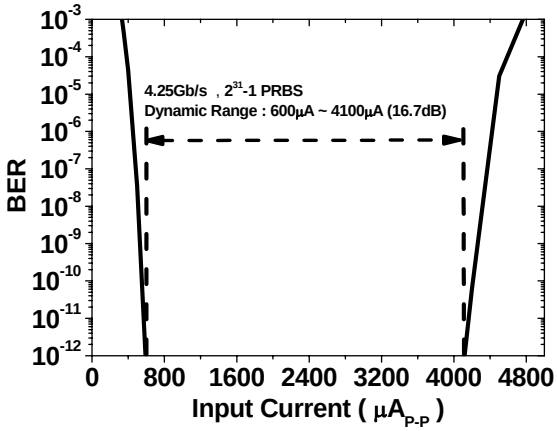

Fig. 5 BER v.s. input current for 2^{31}-1 PRBS at 4.25 Gb/s.

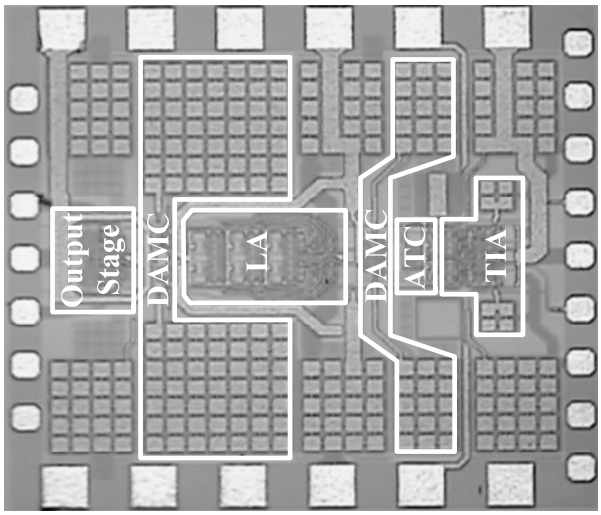

Fig. 6 Chip photograph of the optical receiver.