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G-5-2

Novel MOBILE Circuits Using 3 RTDs Operating up to 12.5 Gb/s

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1. Introduction

After MOnostable-to-BIstable transition Logic Element (MOBILE) was proposed [1], the monolithic integration of RTD and conventional transistors has attracted much attention for high-speed digital circuit application. In spite of MOBILE's merits, three terminal devices in logic circuits using RTD-three terminal devices (HEMT or HBT) integration technology degrade the circuit operation [2]. And integration RTD with three terminal devices needs complicated fabrication process and large areas [3]. To overcome the limit of RTD-three terminal device integration technology, SMOBILE circuit using 2 RTDs [2] and Boolean logic gate using 4 RTDs have been previously reported [4].

In this paper, we propose MOBILE circuits with non-inverted and inverted configuration using only three RTDs. The operations of the proposed circuits were demonstrated up to 12.5 Gb/s. And to demonstrate multi-stage logic operations and to investigate the possibility of the MOBILE circuits using RTDs for future high-speed VLSI applications, two-stage logic circuits were designed and fabricated. The operations of the two stage logic circuits were demonstrated up to 12.5 Gb/s using two-phase clock scheme.

2. Non-inverted and inverted MOBILE using 3 RTDs

Figure 1 (a) shows the circuit configuration of the proposed non-inverted MOBILE circuit, which consists of series-connected RTD pair and RTD resistor pair for monostable-to-bistable transition and current modulation, respectively. The area of the upper RTD is designed to be smaller than that of the lower RTD. The operation principles of MOBILE were previously reported [1]. Figure 1 (b) shows the load line diagram of the input stage. When data is low, the current through input stage is lower than I_{TH} which is the peak current difference of the RTD series pair. When data is high, the current of the input stage is larger than I_{TH}. Thus the proposed circuit functions as non-inverted MOBILE according to its operation principle.

Figure 2 (a) shows the circuit configuration of the proposed inverted MOBILE circuit. The circuit configuration has different input stage compared to non-inverted configuration. There is one more resistor which is biased at the logic high level. Figure 1 (b) shows the load line diagram for the input stage. When data is low, the current through input stage is larger than I_{TH} which is the peak current difference of the RTD pair. When data is high, the current of the input stage is smaller than I_{TH}. Thus the proposed circuit functions as inverted MOBILE according to its operation principle.

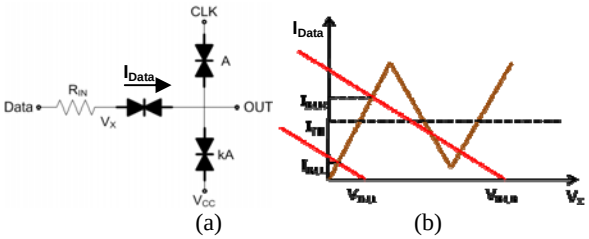


Fig. 1 (a) Circuit configuration for non-inverted output
(b) Load line diagram of non-inverted configuration

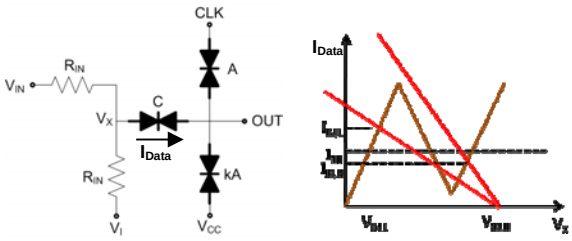


Fig. 2 (a) Circuit configuration for inverted output
(b) Load line diagram of inverted configuration

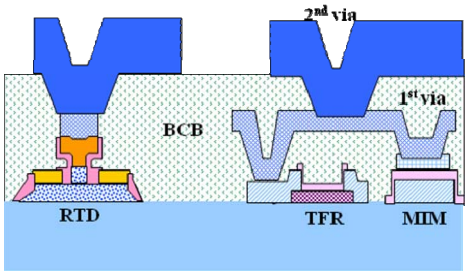


Fig. 3 Cross-sectional view of the fabricated ICs

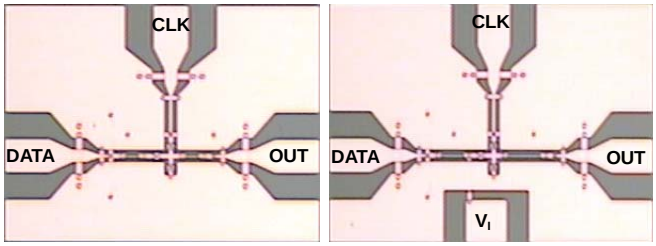
3. Device structure and fabrication

The AlAs/InGaAs/InAs RTD epitaxial layers were grown by MBE and the devices were fabricated using optical lithography, and lift-off process. Figure 3 shows the cross-sectional view of the fabricated ICs. For future VLSI applications, we developed 3-level interconnect system using low-k dielectric BCB.

The peak current density of the fabricated RTDs was 112 kA/cm^2 with a good peak-to-valley current ratio of 12. The peak voltage of the fabricated RTD was 0.3 V.

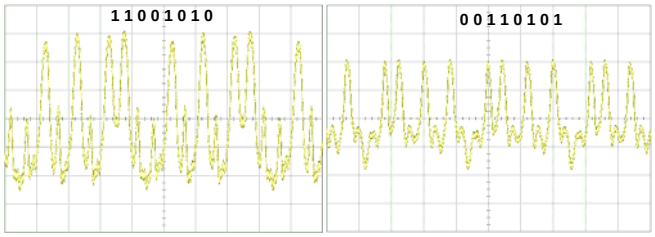
4. Measurement results of the MOBILE circuits

Figure 4 shows the micro-photograph of the fabricated MOBILE ICs. To minimize measurement system effect, we included input/clock buffers in the test circuit. We used simple 50 ohm resistor for input and clock buffers. And 100 ohm resistor for non-inverted circuit and 300 ohm resistor for inverted circuit were used for output buffer.



(a) Non-inverted (b) Inverted

Fig. 4 Microphotograph of the fabricated ICs



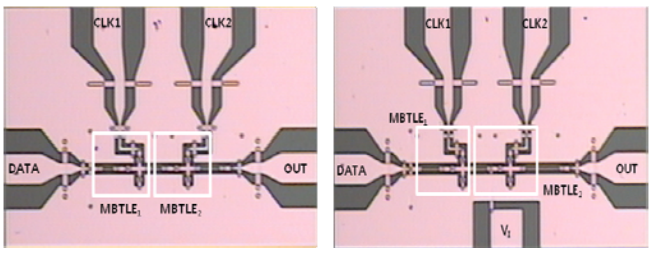
(a) Non-inverted (b) Inverted

Fig. 5 Measurement result at 12.5 Gb/s

In order to demonstrate the operation of the fabricated D-F/F circuit at 12.5 Gb/s, a pulse pattern generator (Anritsu-MP1763B) was used to obtain the data stream and clock. The output of the fabricated circuit was fed into a digital communication analyzer (Agilent 83484A). Figure 4 shows the output bit stream at 12.5 Gb/s with an input bit pattern of (11001010). Figure 5 (a) shows the non-inverted output bit stream and Fig. 5 (b) shows the inverted output bit stream. As shown in the figures, the proper operations of the proposed MOBILE circuits were confirmed at 12.5 Gb/s.

5. Multi-stage operation

To demonstrate multi-stage logic operations and to investigate the possibility of the proposed MOBILE circuits using RTDs for future high-speed VLSI applications, two-stage logic circuits with non-inverted/non-inverted configuration and non-inverted/inverted configuration were designed and fabricated. Figure 6 shows the fabricated two stage logic circuits. For proper logic operation, we use two phase clock scheme to insure input/output isolation as shown in Fig. 7. Figure 8 shows the output bit stream at 12.5 Gb/s with an input bit pattern of (11001010). The measurement results confirm the proper operation of the two stage logic circuits and the possibility of multi stage operation using multi phase clock scheme.



(a) Non-inverted/non-inverted (b) Inverted/inverted

Fig. 6 Microphotograph of the fabricated ICs

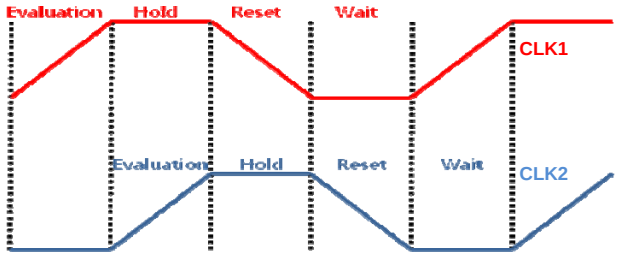
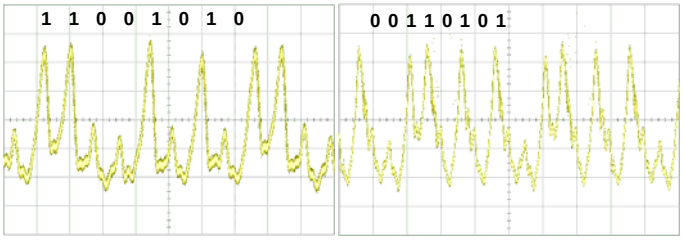


Fig. 7 Two phase clock scheme for two stage operation



(a) Non-inverted/non-inverted (b) Inverted/inverted

Fig. 8 Measurement result at 12.5 Gb/s

6. Conclusion

A new MOBILE circuit using only three RTDs is proposed and fabricated. The operations of the fabricated circuits were confirmed up to 12.5 Gb/s. To demonstrate multi-stage logic operations and to investigate the possibility of the proposed MOBILE circuits using RTDs for future high-speed VLSI applications, two-stage logic circuits with non-inverted/non-inverted and non-inverted/inverted configuration were fabricated and the operation of the fabricated circuits were confirmed up to 12.5 Gb/s. By implementing logic gates using only RTDs, we can reduce circuit complexity and chip area with simple fabrication process. This result indicates the great potential of the proposed circuit for high-speed and low-power digital IC applications. And the applications of MOBILE using RTDs for multi-valued logic and threshold logic will be investigated more deeply in the future.

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