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Silicon oxide Gate Dielectric on N-Type 4H-SiC Prepared by Low Thermal Budget Anodization Method

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1. Introduction

Silicon carbide (SiC) attains much interest because of its excellent physical properties[1]. Since SiC is much more chemically stable than Si, higher oxidation temperature of ~1175°C is required to form silicon dioxide (SiO_2) layers from SiC [2]. It is reported that due to high temperature oxidation, carbon is accumulated at SiO_2/SiC interfaces [3], resulting in deterioration of interfacial properties. In the present study, a low temperature SiC oxidation method at room temperature has been developed using the anodization method in deionized (DI) water. Capacitance-voltage (*C-V*) and current-voltage (*I-V*) characteristics of the obtained SiO_2 devices were demonstrated. Both the inversion current and *C-V* hysteresis is used to reflect the interfacial property [4]. Furthermore, the conduction mechanisms in positively and negatively biased regions are explored by the temperature responses of MOS capacitors.

2. Experiment

Three 4H-SiC wafers with a nitrogen-doped n^- epi-layer on n^+ substrate purchased from CREE Research Inc. were used. The wafer was 8.03° off orientated with a resistivity of 0.02Ω · cm. The thickness and doping concentration of the epi-layer were 10μm and 2.6×10^{15} cm^{-3}, respectively. The initial wafer was cleaned sequentially with two cleaning recipes: H_2SO_4:H_2O, (2:5:1) with temperature>80°C for 5 min and H_2O:HF:$CH_3CH(OH)CH_3$ (100:3:1) for 100s followed by DI water rinsing. Thin SiO_2 layers (27~50Å) were grown on SiC by anodization in DI water with varying grown time. Platinum plates were used as the cathode. The anode was performed by the another platinum plate that was carefully contacted with the backside of the SiC wafer to obtain a uniform anodization field. Postoxidation annealing was implemented in the rapid thermal anneal at 850 °C in N_2 for 10 s. After Al deposition, the 2.25×10^{-4} cm^2 Al gate was defined by conventional photolithography and wet etching. The underside of each wafer was coated with an aluminum film to form MOS capacitors.

3. Results and Discussion

Fig. 1 shows the plot of the capacitance equivalent thickness (CET) of SiO_2, calculated from accumulation capacitance, versus the anodization time. The plot is almost linear, indicating that the interfacial reaction is the rate-determining step. Diffusion of hydroxyl atoms proceeds smoothly, probably due to their small size. The high-frequency (100KHz) *C-V* curves are plotted in Fig. 2. The *C-V* hysteresis is originated from the polarization of interface traps by charging and discharging during bidirectional sweep. Slight hysteresis suggests a satisfactory interfacial quality. Effective oxide charge density on the order of $10^{12}cm^{-2}$ is comparable with that reported by H. R. Lazar *et al*.[5]. Gate current density versus gate voltage (J_G-V_G) relationship is demonstrated in Fig.3. The effective oxide breakdown field in positively biased region, i.e., accumulation region, calculated by using CET is around 5.5~6.7 MV/cm, which is comparable with Si_3N_4 on 4H-SiC [6]. To further identify the conduction mechanism of SiO_2 grown by anodization method, the negative biased J_G-V_G curves measured at high temperatures for CET=33 Å are shown in Fig. 4. The saturated current behavior indicates that the gate currents at evaluated temperatures are limited by minority carrier generation rate. The relationships between log (J_G) at -1V and log (n_i) are examined in Fig. 5. Here, n_i was calculated by theoretical equations [7]. As can be seen, the correlation coefficient is 0.989, which indicates that J_G is directly proportional to n_i. It is inferred that negatively biased J_G is conducted by recombination process. The positive conduction mechanism from the experimental data may be done by using the measured slope of ln(*J*) v.s $V^{1/2}$ as shown in Fig. 6. The extracted slope β determined from Fig. 7 is 1.89×10^{-5} eV $V^{-1/2}m^{1/2}$. The experimental value of β is closer to the calculated $\beta_{Schottky.}$ Hence, it is suggested that the positive conduction mechanism is mainly controlled by Schottky emission. Detailed calculation can be found in [8].The energy band diagrams showing the negative and positive conduction mechanism are illustrated in Fig. 7 (a) and Fig.7 (b) respectively.

4. Conclusions

Silicon oxide on 4H-SiC prepared by low thermal budget anodization method is demonstrated. The oxidation technique seems to be satisfactory, with oxide breakdown strengths greater than 5 MV/cm and slight *C-V* hysteresis. As opposed to the high thermal oxidation temperature, anodization technique can be performed at room temperature.

Acknowledgements

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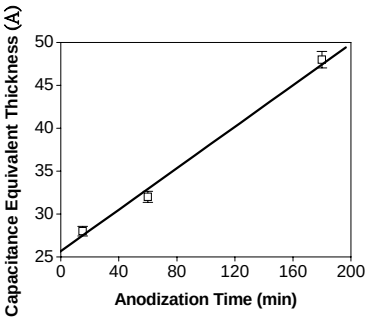

Fig.1. Plot of the CET of SiO_2 on the 4H-SiC substrate using the anodization method vs. the anodization time in DI water. The linear plot indicates that thick SiO_2 layers can be formed by an increase in the anodization time.

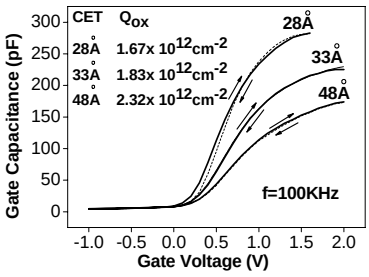

Fig.2. *C-V* curves measured at room temperature of SiO_2 on 4H-SiC fabricated by anodization with varied CET for bidirectional sweep. Negligible hysteresis phenomenon indicates satisfactory interfacial quality.

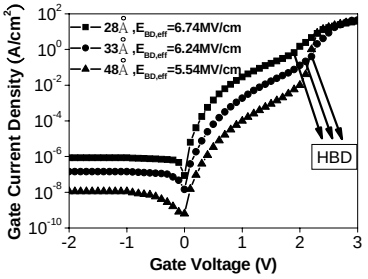

Fig.3. *J-V* curves measured at room temperature of SiO_2 on 4H-SiC with varied CET.

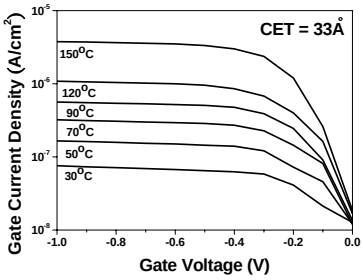

Fig.4. *J-V* curves of SiO_2 on 4H-SiC fabricated by anodization method operated in negatively biased region for different temperatures. The current levels keep saturation and increase with temperatures.

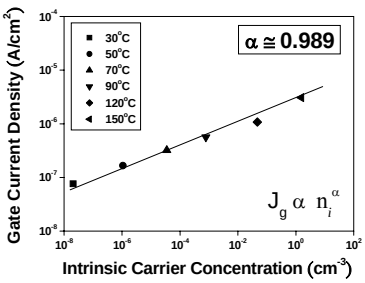

Fig.5. Negatively biased gate current density versus intrinsic carrier concentration for different temperature. The correlation coefficient of 0.989 in log-log scale indicates that gate current is controlled by intrinsic carrier concentration.

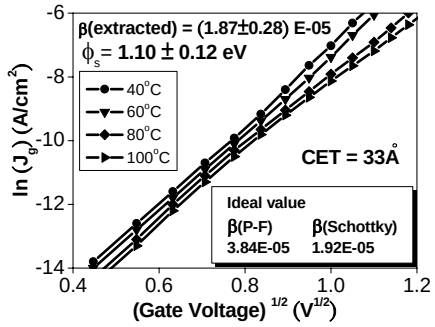

Fig.6. Relationships between gate current density and square root of gate voltage at different temperatures. Extracted slopes β are closer to the calculated $\beta_{schottky}$ value. The Schottky barrier height extracted from the intercept is 1.10eV.

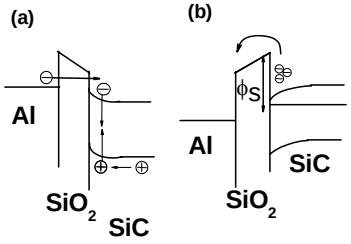

Fig.7. (a) Negatively biased band diagram illustrates the main conduction mechanism of recombination process(b)Positively biased band diagram illustrates the main conduction mechanism of Schottky emission.