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Growth of InAs Channel HEMT Structure on Si substrate and It's Possible Application for Low Power Logic

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1. Introduction

Integration of III-V semiconductors on Si substrates has been investigated for microwave and millimeter-wave devices and monolithic integrated circuits in the past.[1-3] The use of GaAs-on-Si to replace GaAs substrate has the following advantages: high thermal conductivity, potential wafer-size expansion, mechanical hardness of substrates, and lower cost for Si substrates.[3-5] And recently there's a great interest of integrating III-V on Si substrate for low power logic application. High-electron-mobility transistors (HEMTs) with InAs channel layer using antimony (Sb)-based buffers have been studied in recent years.[6-10] The InAs layer was chosen as the channel material for the HEMT due to its high electron mobility and high quantum confinement in the channel region. In this paper, the growth of the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT on Si substrate for high speed electronic application is studied.

2. Experiment

There are two problems to be overcome for the growth of high-quality $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT epitaxial layers on Si substrate. One is the strain induced by the large lattice mismatch of 11 % between the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure and the Si substrate, the other is the residual stress due to the large difference in the thermal expansion coefficients of these two material systems[11]. To obtain high-quality $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT on Si, two buffer layers of Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$ and $Al_{0.5}Ga_{0.5}Sb$/AlSb/GaAs were used. First, the Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$ layer was used as the buffer layer for the growth of GaAs on Si substrate, because Ge and GaAs have similar lattice constants and thermal expansion coefficients.[11] Then, the $Al_{0.5}Ga_{0.5}Sb$/AlSb layers were grown to accommodate the strain induced by the large lattice mismatch between the $Al_{0.5}Ga_{0.5}Sb$/InAs system and the GaAs layer.[10] The $Al_{0.5}Ga_{0.5}Sb$/InAs structure grown on Si is as shown in Figure 1.

A Si (100) substrate wafer with 6^0 off-cut toward the [110] direction and three epitaxial growth systems were used for the growth of the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure on Si in this study. First, an ultra-high vacuum chemical vapor deposition (UHV/CVD) system was used to grow the Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$ layers. Then, a thin GaAs film was grown by a commercial metal organic chemical vapor deposition (MOCVD)[11]. Finally, the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure was grown by a molecular beam epitaxy (MBE) system.

GaSb	3 nm
$Al_{0.5}Ga_{0.5}Sb$	13 nm
InAs	15 nm
$Al_{0.5}Ga_{0.5}Sb$	50 nm
GaSb/AlSb	(2.5 nm/2.5 nm) × 10
$Al_{0.5}Ga_{0.5}Sb$	1 μm
GaSb/AlSb	(2.5 nm/2.5 nm) × 10
AlSb	100 nm
GaAs	2.5 μm
Ge	1 μm
$Si_{0.05}Ge_{0.95}$	0.8 μm
$Si_{0.1}Ge_{0.9}$	0.8 μm
Si substrate	

Fig. 1. The structure of the AlGaSb/InAs HEMT grown on the Si substrate.

For the Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$ layers growth, the Si substrate was first cleaned by 10% HF dipping and then went through high-temperature baking at 800^0C in the growth chamber for 5 minutes. Then, a 0.8μm $Si_{0.1}Ge_{0.9}$ layer, a 0.8μm $Si_{0.05}Ge_{0.95}$ layer, and a 1.0μm Ge layer were grown at 400^0C in sequence on the Si wafer as the buffer layer.[11] After that, a 1.5μm GaAs layer was grown on Ge at a temperature of 600^0C by MOCVD. Finally, the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT was grown on top of the Ge layer by MBE system. The growth of the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure can be divided into two major parts: buffer layer growth and InAs channel layer growth. The growth of the buffer layers includes a GaAs layer, an AlSb layer, two GaSb/AlSb supperlattice and two $Al_{0.5}Ga_{0.5}Sb$ layers, the buffer layers were grown before the channel region growth to accommodate the 7% lattice mismatch between the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure and the Ge layer. The growth temperature of the buffer layers was set at 560^0C. A 1 μm GaAs layer was grown on Ge first. After that, a 100nm AlSb layer, a superlattice of 50nm with 10 pairs of GaSb/AlSb and a 1μm $Al_{0.5}Ga_{0.5}Sb$ were grown layer by layer. Then, 50nm GaSb/AlSb superlattice (10 pairs), a 50nm $Al_{0.5}Ga_{0.5}Sb$ layer, a 15nm InAs layer, a 13nm $Al_{0.5}Ga_{0.5}Sb$ layer and a 3nm GaSb layer were grown. To obtain good quality InAs channel layer, the growth temperature was set at 520^0C after the growth of the

$Al_{0.5}Ga_{0.5}Sb$ layer. The growth rate of InAs channel layer was 1.5Å/s, and the 13nm $Al_{0.5}Ga_{0.5}Sb$ layer and the 3nm GaSb layer are the Schottky layer and the cap layer respectively[11]. The $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT on Si structure grown is as shown in Figure 1.

3. Results and Discussion

Because the $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ interface can be used to accommodate the strain induced by the large lattice mismatch, the upwardly propagated dislocations were bent sideward and terminated very effectively at the $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$ interfaces. Figure 2 presents the TEM micrograph of the InAs layer. As can be seen in this figure, the defect density in the InAs layer was very low.

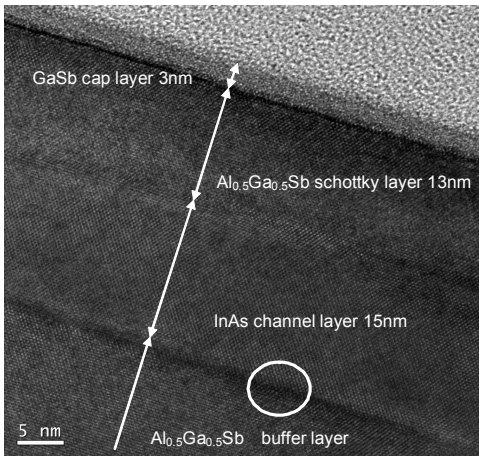

Fig. 2. Cross-section of the TEM images of the InAs layer in the AlGaSb/InAs HEMT

Figure 3 is the X-ray diffraction curve of the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure on Si substrate wafer. The diffraction pattern has seven major peaks and was identified as GaAs, Ge, Si, AlGaSb, InAs, AlSb and GaSb peaks respectively. It indicates that the crystalline quality of the HEMT epitaxial layers is very good. Very high room-temperature electron mobility of 27,300$cm^2/Vsec$ and a sheet density of $3.04 \times 10^{12}/cm^2$ was measured for the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure grown on the Si substrate due to the high quality epitaxial layers grown[13]. It is demonstrated that a very-high-mobility $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure can be grown on Si substrate with properly designed $Al_{0.5}Ga_{0.5}Sb$/AlSb/GaAs and SiGe buffer layers.

4. Conclusions

The cross-sectional TEM images of the AlGaSb/InAs HEMT on Ge show very smooth interfaces for the structure grown and very low defect density for the InAs channel layer. The X-ray diffraction patterns of the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure on Si substrate wafer clearly exhibited seven major peaks and the diffracted peaks indicated that the crystalline quality of the HEMT structure was very good. The room-temperature electron mobility of 27,300$cm^2/Vsec$ and a sheet density of $3.04 \times 10^{12}/cm^2$ were achieved for the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT grown on Si substrate using $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ as the buffer layer. This is the highest mobility for a HEMT structure grown on Si substrate reported so far and we have successfully demonstrated for the first time that a very-high-mobility $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure can be grown on Si substrate if the buffer layers are properly designed. Recent studies have shown that InAs HEMT with submicron gate length has shown very promising DIBL, Ion/Ioff, gate delay characteristics for logic applications. Current study with high mobility InAs HEMT structure on Si could be applicable to this application if proper process integration sequence and epi materials are designed.

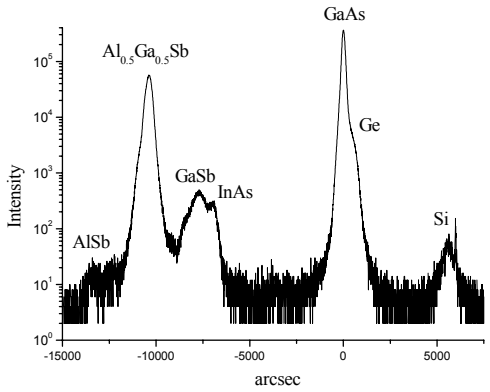

Fig. 3. The double crystal X-ray diffraction patterns

Reference

[1] Guang-bo Gao, Zhi-fang Fan, D. L. Blackburn, M. S. Ünlü, J. Chen, K. Adomi, and H. Morkoc, Appl. Phys. Lett. 58, 1068 (1991).

[2] Kai Ma, Ray Chen, David A. B. Miller, and James S. Harris, Jr., IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS 11, 1278 (2005).

[3] Mitsuhiko Goto, Yasumitsu Ohta, Takashi Aigo, and Akihiro Moritani, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES 44, 668 (1996).

[4] K. Ohtsuka and H. Nakanishi, in Proc. 19th Int. Symp. Gallium Arsenide and Related Compounds, 881 (1992).

[5] T. Aigo, H. Yashiro, A. Jono, A. Tachikawa, and A. Moritani, Electronics Lett. 28, 1737 (1992).

[6] J. Brad Boos, Walter Kruppa, Brian R. Bennett, Doewon Park, Steven W. Kirchoefer, Robert Bass, and Harry B. Dietrich, IEEE TRANSACTIONS ON ELECTRON DEVICES 45, 1869 (1998).

[7] N. A. Papanicolaou, B. R. Bennet, J. B. Boos, D. Park and R Bass, ELECTRONICS LETTERS 15th 41, September 2005.

[8] KANJI YOH, TOSHIAKI MORIUCHI, and MASATAKA INOUE, IEEE ELECTRON DEVICE LETTERS 11, 526 (1990).

[9] C. R. Bolognesi, E. J. Caine, and H. Kroemer, IEEE ELECTRON DEVICE LETTERS 15, 16 (1994).

[10] R. Tsai, M. Barsky, J. Lee, J. B. Boos, B. R. Bennett, R. Magno, C. Namba, P. H. Liu, A. Gutierrez, and R. Lai, IEEE, 276 (2002).

[11] Y. C. Lin, H. Yamaguchi, E. Y. Chang, Y. C. Hsieh, M. Ueki, Y. Hirayama, and C. Y. Chang, APPLIED PHYSICS LETTERS 90, 023509 (2007).