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N-channel MOSFETs with *In-situ* Silane-Passivated Gallium Arsenide Channel and CMOS-Compatible Palladium-Germanium Contacts

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1. Introduction

Research on new channel materials other than Si is being actively pursued owing to their high carrier mobilites for potential applications in high performance CMOS logic beyond 22 nm technology node. Germanium is a promising channel material for p-FETs due to high hole mobility whereas III-V compound semiconductor materials with high electron mobility are attractive for n-FETs. Due to advantages such as high melting point and large bandgap, GaAs receives more attention than other III-V candidates for n-FETs applications. However, there are several difficulties in the process integration of well-tempered GaAs MOSFETs. The lack of high quality and thermodynamically stable insulators to prevent Fermi-level pinning and reduce interface states [1], the limitations to achieve high dopant activation [2],[3] and the formation of low resistance CMOS-compatible contacts [4] are the most important integration issues. In addition, common contact technologies to GaAs employing gold (Au) should not be used for CMOS-compatibility.

In this paper, we report a novel n-channel GaAs MOSFET structure integrating *in-situ* silane (SiH_4) passivated gate stack, Si and P co-implanted S/D regions, and CMOS compatible palladium-germanium (PdGe) ohmic contacts for the first time.

2. Device Fabrication

The process sequence for device fabrication is depicted in Fig. 1. P-type Zn-doped GaAs (100) substrates with a doping concentration of $1\text{-}5\times10^{16}$ cm^{-3} were used. Pre-gate clean employed degreasing using acetone and isopropanol, native oxide and elemental As removal using HCl and NH_4OH, and surface passivation using $(NH4)_2S$ solution [5]. After cleaning, the wafers were loaded into a MOCVD system, where *in-situ* vacuum anneal at 600˚C, SiH_4 treatment and high-κ dielectric deposition were carried out. Post deposition anneal (PDA) at 500˚C for 60 s was then performed. After reactive sputter deposition of TaN metal gate and gate patterning, Si and P co-implantation was performed at a dose of 1×10^{14} cm^{-2} and 5×10^{13} cm^{-2} respectively, followed by S/D dopant activation at 850˚C for 10 s. Low resistance PdGe ohmic contacts were formed after annealing at 340˚C for 1 min to complete the fabrication process.

3. Results and Discussion

A. Silane Surface Passivation for Gate-Stack Formation

First, we explore the use of HfO_2 as a high-κ gate dielectric to form MOS capacitors. In Fig. 2, XPS spectra of As 3*d* and Ga 3*d* show that the formation of native oxide can be successfully prevented, i.e. GaAs surface can be effectively passivated, by doing a vacuum anneal at 600˚C and an additional SiH_4 treatment. The Si interfacial layer was fully oxidized in the subsequent process as only Si-O bond (103.5 eV) signal was detected in the Si 2*p* spectrum. In Fig. 3, the steeper *C-V* characteristics of capacitors with SiH_4 passivation indicate the effective reduction of interface state densities D_{it}. Based on conductance method, D_{it} of capacitors without pre-treatment, with vacuum anneal only and with both vacuum anneal and SiH_4 treatment were extracted to be about 1×10^{13}, 8×10^{11}, and $4\times10^{11}$$cm^{-2}eV^{-1}$, respectively. High-resolution TEM images (Fig. 4) show better interfacial morphology with SiH_4 treatment, suggesting effective suppression of Ga and/or As oxide formation during subsequent high temperature processes.

B. n-MOSFETs with HfAlO gate dielectric

Although HfO_2 can be integrated in MOS capacitors, it suffers from thermal instability during S/D dopant activation. Therefore, HfAlO dielectric was chosen for integration in n-MOSFETs. Fig. 5 (a) and (b) show cross-section and layout of the GaAs n-MOSFET. TEM images of PdGe contact and gate stack are shown in Fig. 5 (c) and (d), respectively. *I-V* characteristics of the PdGe contacts in Fig. 6 demonstrate excellent ohmic behaviour. Extraction based on averaged over three TLM sites indicates low contact resistance of the devices (Fig. 7), which can contribute to better device performance due to significant reduction in series resistance. In Fig. 8, excellent rectifying diode characteristics with more than five orders on/off ratio at a bias of ±1V and slope of ~67.8mV/decade in the forward bias region were observed in the Si + P co-implanted n+/p junction. Fig. 9 shows the *C-V* characteristics of the transistor with S/D shorted with substrate. The EOT of the device with 19.6 nm of HfAlO ($\kappa \approx 16.8$) is about 4.5 nm.

I_{DS}-V_{GS} and G_m-V_{GS} characteristics of the GaAs n-MOSFET are shown in Fig. 10. For gate overdrive of 1V and V_{DS} of 1.2V, the GaAs transistor with width of 100 μm provides a drain current of 0.45 mA. The I_{DS}-V_{DS} characteristic of a GaAs n-MOSFET with 3 μm gate length and 100 μm width is plotted in Fig. 11 at various gate overdrives, demonstrating good behavior. Comparing to recently reported p-doped GaAs n-MOSFETs with a gate length of 4 μm and EOT of about 2-3 nm [6], the n-channel transistors in this work demonstrate more than three orders magnitude higher in drive current performance. This is possibly due to the significant reduction in series resistance as a result of lower resistance at the PdGe contacts and higher S/D dopant activation with additional P implantation. Since Si is amphoteric in the GaAs crystal, the additional Group-V P is used to suppress the generation of Ga on arsenic site (Ga_{As}) acceptors and Si on arsenic site (Si_{As}) acceptors, resulting in much higher Si occupancy in gallium sites [3].

4. Conclusion

A novel *in-situ* SiH_4 passivation method was demonstrated for the formation of high-quality gate stacks on GaAs. A self-aligned GaAs n-MOSFET comprising *in-situ* SiH_4 passivated gate stack was fabricated, Si + P co-implanted S/D regions and CMOS compatible PdGe ohmic contacts were demonstrated for the first time. *In-situ* SiH_4 passivation replaced the native oxide with a stable thin SiO_2 interfacial layer, providing gate stack with higher thermal processing capability and lower interface trap densities. Additional P implantation together with PdGe ohmic contacts provides highly activated n+ S/D regions with low resistance ohmic contacts, which can significantly reduce the series resistance and increase the device performance.

Acknowledgements

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References

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- Pre-gate Clean
- *In-situ* Passivation (Vacuum Anneal→SiH_4 Treatment) and High-κ Dielectric Deposition
- Metal Gate (TaN) Deposition
- Gate Patterning
- Si + P Co-implantation and RTA
- Contact Patterning and Contact Metal (Pd/Ge) Deposition
- Lift-off and Contact Formation

Fig. 1. Process flow for fabrication of the first GaAs n-MOSFETs with SiH_4 passivation, Si+P co-implanted S/D, and CMOS-compatible contact technology.

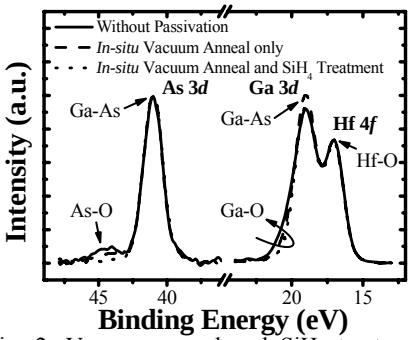

Fig. 2. Vacuum anneal and SiH_4 treatment effectively eliminate native oxide formation, as shown by XPS spectra of As 3*d* and Ga 3*d*.

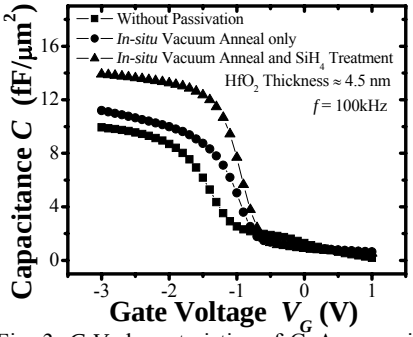

Fig. 3. *C-V* characteristics of GaAs capacitors. Vacuum anneal and *in-situ* SiH_4 passivation reduces the interface state densities.

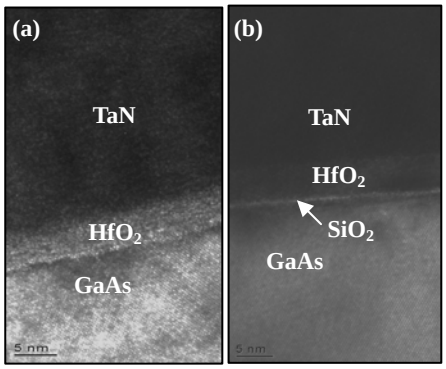

Fig. 4. HRTEM images of the TaN/HfO_2/GaAs gate stacks (a) with vacuum anneal only and (b) with both vacuum anneal and SiH_4 treatment.

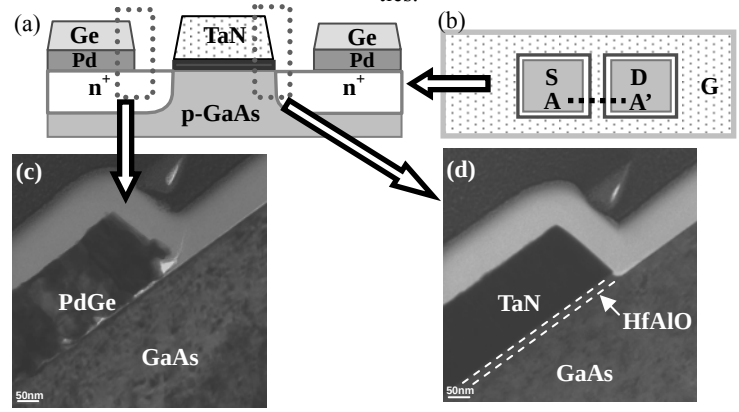

Fig. 5. (a) Device cross-section along a line A-A' as shown in (b) the top view of a GaAs n-MOSFET. TEM images showing (c) contact region and (d) gate stack of the transistor.

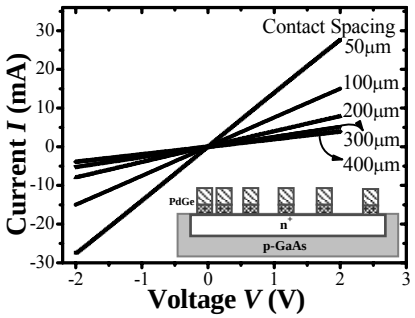

Fig. 6. *I-V* characteristics showing excellent ohmic behaviour of PdGe contacts on the n^+ GaAs region at various spacing on the TLM structure shown in the inset.

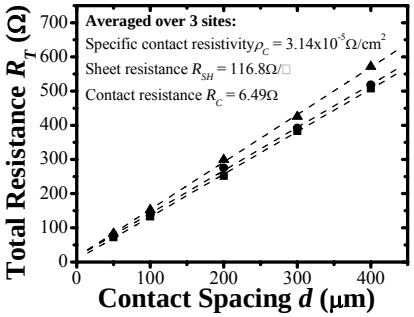

Fig. 7. Total resistance as a function of contact spacing for three TLM sites. The low contact resistance of the device enhances the device performance in this work.

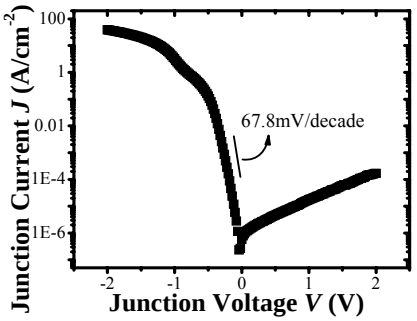

Fig. 8. Excellent rectifying diode characteristic with more than five orders on/off ratio at a bias of ±1V was observed in the Si + P co-implanted n+/p junction.

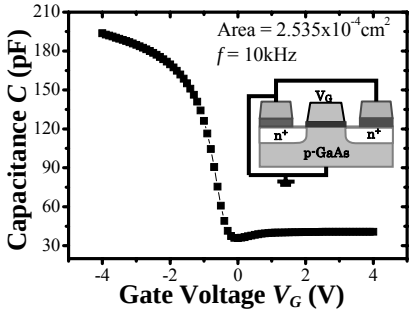

Fig. 9. *C-V* characteristic of a n-channel GaAs transistor with Silane-passivated surface showing low interface state density.

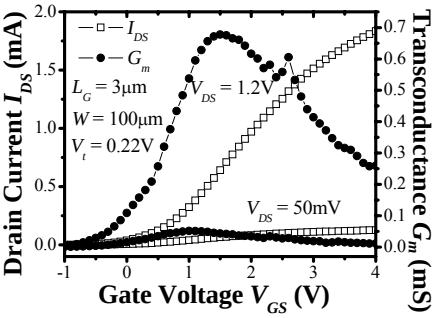

Fig. 10. A GaAs n-MOSFET featuring *in-situ* SiH_4 passivation scheme, Si + P co-implantated S/D and CMOS compatible PdGe ohmic contacts, demonstrating good I_{DS}-V_{GS} and G_m-V_{GS} characteristics.

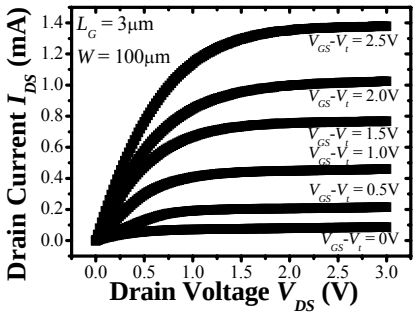

Fig. 11. I_{DS}-V_{DS} characteristic of a GaAs n-MOSFET with a gate length of 3 μm.