Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 1052-1053

G-7-3

Improved electrical characteristics of Pt/Gd_2O_3/GaAs MOS capacitors with surface preparation procedures

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1. Introduction

GaAs metal-oxide-semiconductor (MOS) devices with different high-*k* gate dielectrics have been of more interest in recent years. Examples of these include the highly-concerned Hf-based oxides,[1-4] $(Gd,Ga)_2O_3$,[5,6] Al_2O_3,[7] and TiO_2.[8] The primary bottleneck of these high-*k*/GaAs structures in practical MOSFETs is a large density of interface states (D_{it}), which causes significant Fermi-level pinning effect and other poor electrical properties. Accordingly, manipulation of the chemical bonding configuration at the dielectric/GaAs interface is significant in determining the device performance since the prepared GaAs surface is likely to debase during the dielectric deposition and thermal anneal processing. Nowadays, several groups have demonstrated several promising capacitor[3,4] and transistor[9] characteristics by performing suitable surface preparation techniques, mainly comprising two aspects of the wet-chemical cleaning and the interface passivation,[2-8] respectively. Numerous acidic or basic wet solutions, chemical pretreatments, passivated layer, and the combination of former approaches have been studied in depth. In this study, we demonstrated that improved electrical performances of Gd_2O_3 dielectric thin-films deposited on n-GaAs substrates by optimizing both wet-chemical cleaning processes (WCP) and sulfide passivation conditions. Low gate leakage, hysteresis free and reduced interface state density can be achieved in the fabricated Gd_2O_3/GaAs structures.

2. Experimental

MOS structures were fabricated on Si-doped (~1 x 10^{18} cm^{-3}) n-type GaAs substrates undergoing four different WCPs, as listed in Table 1. We characterized the surface chemistry by employing x-ray photoelectron spectroscopy (XPS) that Al *Kα* is used as an excitation source. The Ga*2p3* and As*2p3* core-level spectra were analyzed by least-square fit assuming components comprising a Gaussian line shape convoluted with a Lorentzian broadening function after subtraction of the background. The Gd_2O_3 thin film was further deposited by e-beam evaporation as the gate dielectric and further densified by annealing at 500°C for 10 s in an Ar/O_2 ambient. Sputtered Pt dots were patterned as circular gate electrodes through the specific shadow mask with the In/Pt backside Ohmic contact. The capacitance–voltage (*C–V*) curves of the fabricated Pt/Gd_2O_3/GaAs MOS capacitors were measured using an HP4284; the value of D_{it} was also estimated by combining conductance–voltage (*G–V*) data.

3. Results and Discussion

Figure 1 presents As*2p3* and Ga*2p3* photoemission spectra after four WCPs; the fitting results of all deconvoluted peaks are also shown and summarized in Table I. It was found that both kinds of native oxides, especially for As_2O_x, were obviously decreased with adding NH_4OH and $(NH_4)_2S$ aqua solutions in GaAs cleaning; moreover, the amount of elemental As due to As_{Ga} antisite defects was also reduced. Suppression of above undesirable components further improves the interface quality during high-*k* film deposition, aiding to achieve the better insulator characteristics, as displayed in Figs. 2 and 3. Poor high-*k* dielectric/GaAs interface leads to the larger frequency dispersion at accumulation capacitance and stronger frequency–dependent *C-V* curves. Therefore, we can qualitatively examine the interface properties through the variation of △C and △V values [Fig. 2(b)] that are defined: $\triangle C(@V_g=3V) = 1 - C(@1MHz) / C(@1kHz)$ and $\triangle V(@C_{FB}) = V_g(@1kHz) - V_g(@100kHz)$, respectively. It was concluded that the WCP — HCl + NH_4OH + Sulfide (1%, 80°C) entirely showed superior electrical performance, including a higher oxide capacitance, negligible hysteresis width, lower leakage current density (J_g) and smaller △C/△V, with the D_{it} of 7 x 10^{12} $cm^{-2}ev^{-1}$, respectively. The Gd_2O_3/GaAs MOS capacitors studied in this work after optimized WCP can exhibit excellent insulating properties with respect to HfO_2 dielectrics reported on n-GaAs in combination with Si or Ge interfacial control layers. In addition, performing diluted $(NH_4)_2S$ immersion at 80 °C benefits to diminish the charge trapping and reduce the J_g; these findings can be reasonably interpreted by abating unstoichiometric GaAs-oxides and As-enriched layer at high-*k*/GaAs interface. Examining the corresponding XPS results in Fig. 4, both As_2O_x and Ga_2O_x have presented on the top of Gd_2O_3 films after 500 °C thermal annealing. The concentration of Ga_2O_x is 13, 6, and 4 % for these three samples with that of As_2O_x below 3 % when we supposed the homogeneous mixing of As_2O_x and Ga_2O_x in Gd_2O_3 bulk. The higher Ga_2O_x concentration was believed to result from the heat reaction: As_2O_3 + GaAs → Ga_2O_3 + 4As. Furthermore, the formation of the by-product As close to interface and subsequent volatilization via high-*k* films may increase the J_g and degrade other electrical properties.

4. Conclusions

The impact of the WCP on the interfacial and electrical characteristics of Pt/Gd_2O_3/GaAs MIS capacitors

has been studied. The hysteresis free, the J_g of 1 x 10^{-6} A/cm^2 @V_g = 1V and the D_{it} of 7 x 10^{12} cm^{-2}ev^{-1}, can be achieved at CET of ca. 20 Å after the WCP optimization.

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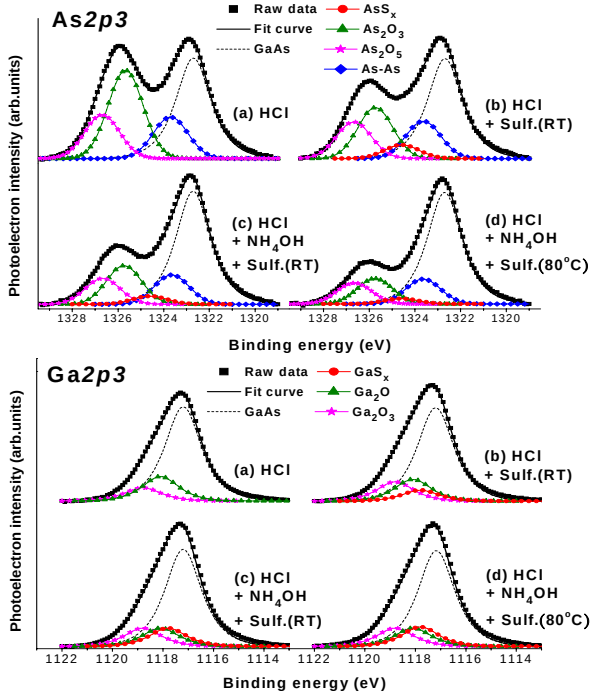
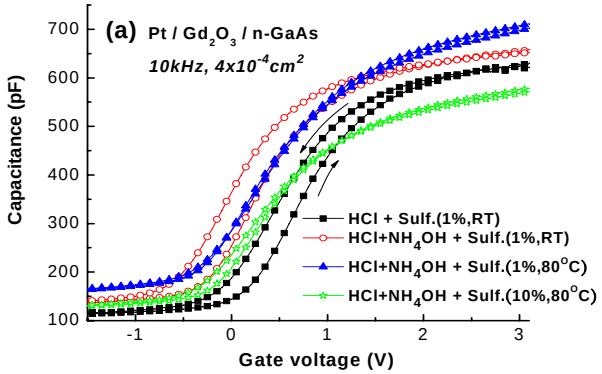


Fig. 1 As*2p3* and Ga*2p3* core-level spectra of GaAs wafer after four WCPs. Note that the cleaned surface was exposed to air for 30 min. Note that the ratio of $(NH_4)_2S$ to H_2O = 1:100.

Wet Clean	As-As/As_{Total}	As-S/As_{Total}	Ga-S/Ga_{Total}	As_2O_x/As_{Total}	Ga_2O_x/Ga_{Total}
HCl	15.4 %	–	–	45.6 %	27.8 %
HCl+Sulf.(RT)	14.9 %	5.4 %	7.3 %	34.8 %	27.6 %
HCl+NH_4OH+Sulf.(RT)	12.8 %	3.5 %	11.7 %	28.1 %	23.5 %
HCl+NH_4OH+Sulf.(80°C)	12.3 %	2.6 %	12.5 %	22.9 %	23.2 %

Table. 1 Chemical ratios calculated by XPS fitting results according to the different WCPs in Fig. 1.



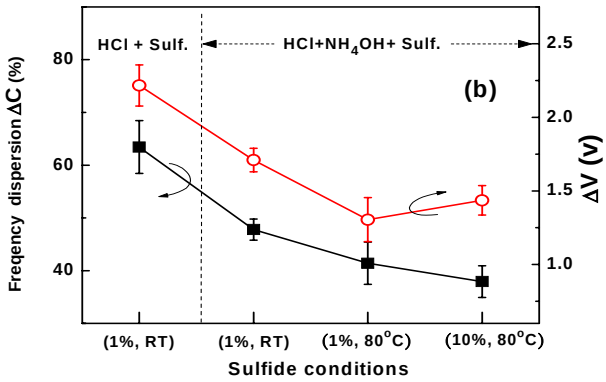


Fig. 2 (a) 10 kHz *C-V* curves and (b) variations of △C and △V values of Pt/Gd_2O_3/n-GaAs capacitors after four different WCPs.

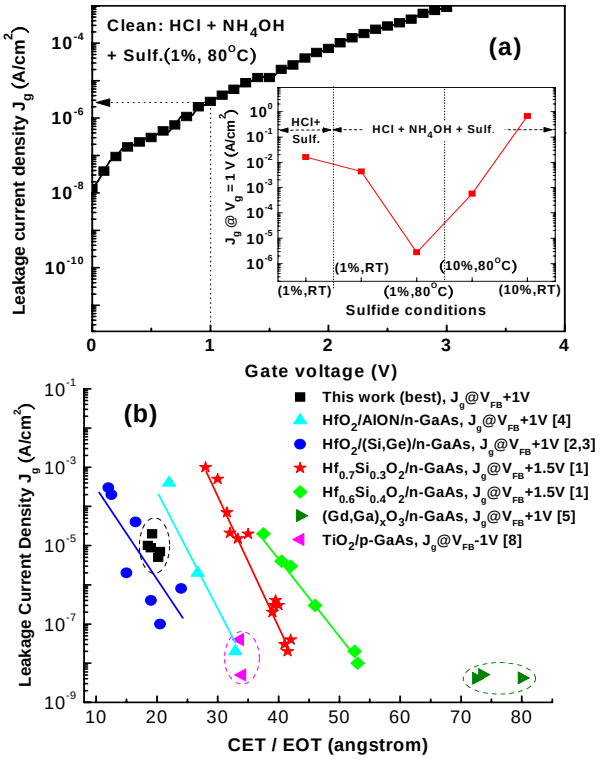


Fig. 3 (a) Gate leakage current curve of Pt/Gd_2O_3/n-GaAs capacitor after the WCP — HCl + NH_4OH + Sulfide (1%, 80 °C). Inset: Comparison of J_g @ V_g = 1V of above devices after various WCPs. (b) Comparison of J_g versus CET or EOT characteristics in this work with other's published data.

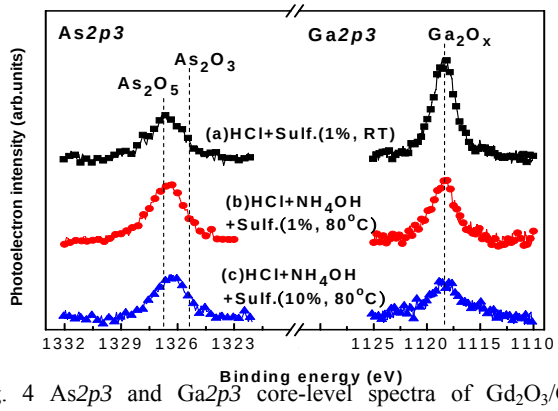


Fig. 4 As*2p3* and Ga*2p3* core-level spectra of Gd_2O_3/GaAs structure after three WCPs.