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Performance and Stability of ZnO/ZnMgO Hetero-MIS FETs

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1. Introduction

Zinc oxide (ZnO) has attracted considerable attention as the one of key materials for the realization of transparent electronics and/or flexible electronics. In contrast to other wide band gap semiconductors such as GaN or SiC, ZnO can be formed at relatively low temperatures. ZnO-based thin film transistors (TFTs) formed on a flexible substrate even at room temperature are demonstrated[1]. So far, we have demonstrated that the use of a heterostructure significantly improves the device performance of ZnO-based TFTs[2, 3]. For practical device applications, the stability of the device operation is important. However, a large hysteresis was observed in the transfer characteristics in devices with an Al_2O_3 gate dielectric[3]. We therefore examined the use of a gate dielectric of HfO_2 for the improvements in the stability as well as in the performance.

2. Growth and device fabrication

The growth of the ZnO/ZnMgO heterostructures was performed using a plasma-assisted molecular beam epitaxy system (EpiQuest) equipped with Knudsen cells for Zn and Mg, and a plasma cell for oxygen radicals operated at 350 W. An *a*-plane sapphire was used as the substrate. A 15 nm thick ZnO layer was grown on the substrate at a low temperature of 250°C, followed successively by a 200 nm thick $Zn_{0.7}Mg_{0.3}O$ layer, a 10 nm thick ZnO channel layer, and a 2 nm thick $Zn_{0.7}Mg_{0.3}O$ cap layer (sample A). The growth temperatures used were 350 °C for the ZnMgO layers and 500 °C for the ZnO channel. All the layers were nominally undoped. The structure without having the cap ZnMgO layer was also grown for comparison (sample B). A high-mobility two-dimensional electron gas (2DEG) is formed in the ZnO channel layer. The 2DEG is induced by the interplay between the spontaneous and piezoelectric polarizations in the heterostructures [4] and was confirmed by the observation of the Shubnikov-de Haas oscillations at low temperatures[5]. The electron mobility and concentration characterized by the van der Pauw method at room temperature were 180 cm^2/Vs and 1.2×10^{13} cm^{-2}, respectively.

Fabrication of the device was carried out using conventional photolithography. Firstly, the device periphery was defined by electron-cyclotron resonance (ECR) plasma etching, using a mixture of CH_4 and CF_4. In order to reduce the plasma-induced damage during the ECR etching in the structure, the thickness of the ZnMgO buffer layer was reduced to 0.2 μm. Ohmic contacts were formed by In (20 nm)/Au (200 nm) evaporation and lift-off. The In/Au layers were formed on top of the ZnMgO cap layer for sample A without exposing the underlying ZnO channel layer. For sample B, the ohmic layers were formed on top of the ZnO channel layer. This fabrication process eliminates the etching of the ZnMgO cap layer for sample A, leading to the formation of a facilitated ohmic contact[3]. The annealing temperature for the ohmic contacts was 400 °C. Finally, the gate dielectric, of either a 50 nm thick Al_2O_3 layer, or HfO_2 layer, and Ti (20 nm)/Au (70 nm) metal layers were formed by electron-beam evaporation and lift-off. Again, the gate dielectric layer is formed either on top of ZnMgO for sample A or on top of ZnO for sample B. A cross-sectional view of the device (sample A with an Al_2O_3 gate dielectric) is depicted in Fig. 1. A hetero-metal-insulator-semiconductor (hetero-MIS) structure is formed for sample A, while a MIS structure is formed for sample B. The channel width of the device was 50 μm, and the gate length was varied between 1 and 50 μm.

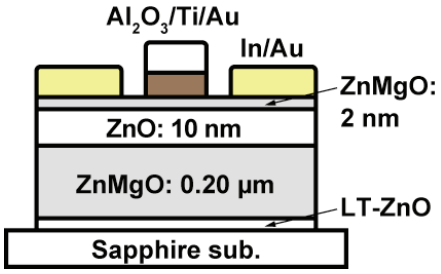

Fig. 1 Cross-sectional structure of a ZnO/ZnMgO hetero-MIS FET.

3. Results and discussion

The drain current versus source-drain voltage (I_D–V_{DS}) characteristics were measured using HP4156A. Fig. 2 (a) and (b) show the I_D–V_{DS} characteristics of 1-μm-long gate devices for gate dielectrics of Al_2O_3 and HfO_2, respectively. The gate voltage V_G was decreased from 1 to –4 V in steps of –1 V. The devices for both gate dielectrics showed good saturation characteristics. The spacing between the source and gate electrodes of the devices was 1 μm, which is decreased by 1 μm compared to those reported in Ref. 3 in order to reduce the access resistance. Therefore, larger transconductance values g_m of 54 and 71 mS/mm compared to that of 28 mS/mm in Ref. 3 were obtained for gate dielectrics of Al_2O_3 and HfO_2, respectively. Because of the higher dielectric constant of HfO_2, a larger improvement in

the g_m was obtained.

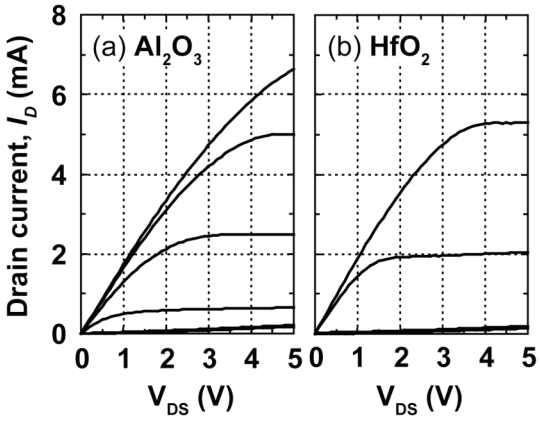

Fig. 2 I_D–V_{DS} characteristics of 1-μm-long gate devices for gate dielectrics of Al_2O_3 (a) and HfO_2 (b), respectively. A larger transconductance was observed for the HfO_2 gate dielectric.

The improvement of g_m by a factor of 2 is brought primarily by the reduction in the access resistance. Therefore, the reduction of the access resistance is crucial for the realization of high-performance ZnO-based FETs. Fig. 3 shows how g_m values depend on the source to gate spacing for Al_2O_3 gate devices. The reciprocal g_m linearly increases as the source to gate spacing increases for gate length of 1 and 2 μm. This verifies that the g_m value can be improved by reducing the source to gate spacing (access resistance).

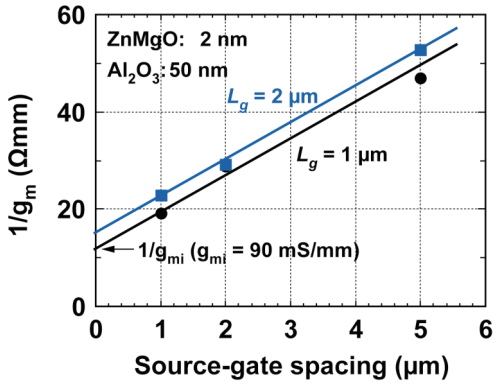

Fig. 3 Reciprocal transconductance $1/g_m$ vs. source-gate spacing for Al_2O_3 gate devices.

The previously fabricated ZnO/ZnMgO hetero-MIS FETs with an Al_2O_3 gate dielectric showed a large hysteresis of about 2 V in the transfer characteristics. The reduction of the hysteresis is crucial for the practical applications of ZnO-based FETs. We thus examined the hysteresis characteristics for both gate dielectrics of Al_2O_3 and HfO_2. The shift of V_T was measured by successively scanning the gate voltage downward and upward between 4 V and -4 V. Fig. 4 summaries the V_T values obtained by downward (circles) and upward (triangles) scans, for both gate dielectrics as a function of gate length. A large V_T shift, of 0.6 V on average, was observed again for Al_2O_3. In contrast, a greatly reduced V_T shift of less than 0.1 V was obtained for HfO_2. The corresponding mobile charge density was 1.4×10^{11} cm^{-2}. Therefore, the use of a HfO_2 gate dielectric enhances the stability as well as the performance of ZnO/ZnMgO hetero-MISFETs. Similar characteristics were observed for the MIS FETs (sample B). However, a current drift was observed for the MIS FETs.

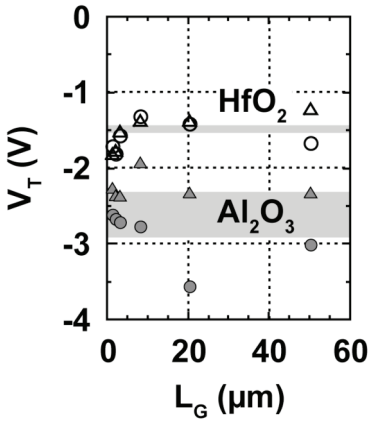

Fig. 4 Hysteresis characteristics for the gate dielectrics of Al_2O_3 and HfO_2.

3. Conclusions

We have demonstrated that significantly improved performance was obtained for ZnO/ZnMgO FETs by reducing the access resistance. We also showed that the use of HfO_2 as the gate dielectric greatly improved the stability. The 1 μm long gate device exhibited transconductance of 71 mS/mm, with a greatly reduced threshold voltage shift of less than 0.1 V. These results have demonstrated the potential for practical applications of ZnO-based FETs, and have indicated their high-performance capability for transparent and flexible electronics.

References

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