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Real-Time Variable-Resolution and Dynamic Range Boosting CMOS Image Sensor

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1. Introduction

In recent years, advance image processing techniques enables many visual functions such as robotic vision, motion detection, target tracking and more to be implemented in an imaging system. Variable-resolution imaging allows for the capturing of the data of interests and can reduce computational complexity. There are many ways to vary spatial resolution in an image, for example, using software algorithm, digital circuits [1] and analog circuits [2-4]. In this work, the proposed new method can realize variable resolution imaging system through analog averaging circuits. This new scheme can also reduce FPN and extend the dynamic range of pixel by operating under different integration lengths. We propose a new operation scheme which requires only simple control signals with the modified CDS (Correlated Double Sampling) circuit in conventional CIS pixel arrays.

2. Design and Operation

CDS circuit is usually used to extract the output signal of a pixel by canceling the offset voltage of the operational amplifier (OPA) and obtaining differential voltage between reset and signal levels [5].Two extra capacitances (C_{TEMP1}, C_{TEMP2}) are added to a conventional CDS circuit, and they are isolated by a switch, as shown in Fig.1. Three operation modes, normal mode, variable resolution mode and dynamic range boosting mode, are avaiable in this system.

Normal mode

In normal mode, C_{TEMP1} and C_{TEMP2} are disabled; this circuit functions as a typical CDS. The timing diagram for this operation is shown in Fig.2. OPA is reset during phase A, and OPA obtains output signal during phase B. The output signal can be expressed by eqn.(1). In this operation mode, the output signal of each pixel is directly amplified by a capacitance ratio.

$$\Delta V_{out} = -\left(\frac{C_{in}}{C_F}\right)\times \Delta V_{in} \quad (1)$$

Variable resolution mode

In order to give a clear illustration of operating principle, four 3-T pixels array, two proposed CDS circuits are used as a example shown in Fig.3.When C_{TEMP1} and C_F are assigned to be equal to C_{in}, and C_{TEMP2} is isolated. In variable resolution mode, the signals of odd row are stored in C_{TEMP1}, which is to be averaged with even row data. The timing diagram is shown in Fig.4. During phase A, the operation is as same as normal mode, the output signal equals to eqn.(1). The output signal $\triangle V_{out1}$ equals to $-\triangle V_{in1}$, are then stored in the C_{TEMP1} during phase B.

Capacitance Averaging: The signal of even row is read out during phase C, as same as phase A. During phase D, C_{TEMP1} shunts with C_F, the charges in the C_{TEMP1} ($\triangle V_{out1}\times C_{TEMP1}$) and C_F ($\triangle V_{out2}\times C_F$) are redistributed. The output signal can be expressed by eqn.(2). Because C_{TEMP} and C_F equal to C_{in}, and $\triangle V_{out}$ will equal to (1/2)×($\triangle V_{out1}$+$\triangle V_{out2}$). By this principle, the proposed CDS provides the average voltage of odd and even rows in the same column immediately.

$$\Delta V_{out} = \frac{\Delta V_{out1}\times C_{TEMP1} + \Delta V_{out2}\times C_F}{C_F + C_{TEMP1}} \quad (2)$$

Resistance Average: Following above steps, the proposed CDS circuit achieves the averaging of the output signals from two rows. An average voltage of two columns through resistance averaging can be obtained as well. During phase D, the output node ($V_{sub\text{-}out1}$) becomes the average voltage of four pixels.

Dynamic Range Boosting

In this mode, C_{TEMP2} is set to shunts with C_{TEMP1}, where C_{TEMP2} is equal to 2/3 C_{TEMP1}.

There are long (T_1) and short (T_2) integration periods in the timing control. The signal of T_1 will be stored in C_{TEMP} (C_{TEMP1} and C_{TEMP2}), and CDS circuit merges two signals at the end of the different integration periods. The timing diagram is as shown in Fig.5. The output signal can be expressed by eqn.(3). The output signal can be written as eqn.(4) according to our previous assumptions. The signals of T_1 and T_2 occupy about 62.5% and 37.5 % of full output swing, respectively. And the dynamic range can be extended by $20\log(T_1/T_2)$ [6].

$$\Delta V_{out} = \frac{\Delta V_{out1}\times C_{TEMP} + \Delta V_{out2}\times C_F}{C_F + C_{TEMP}} \quad (3)$$

$$= 0.625\Delta V_{out1} + 0.375\Delta V_{out2} \quad (4)$$

3. Experimental Results

The performance of the proposed architecture is evaluated by a 128×128 CMOS image sensor array realized by 0.35μm 2P4M logic technology. To measure the averaging output of this circuits, one of input signal is held at zero, and the other end is swept from 0 to 1.6V (the maximum output swing of a pixel). Fig.6 shows the measured averaging result of CDS and resistor circuits, respectively. The measured results show that the CDS averaging circuit induces at most 3.3% error, while the resistor circuit leads to a maximum error of 1.6%. Fig. 7 shows two images captured under normal and low resolution modes, where the averaging effect is clearly shown. The measured optical responses of normal and dynamic range boosting modes a single pixel is compared in Fig. 8. By setting T_1=682ms and T_2=5.2ms, a dynamic range extension of 42 dB are successfully demonstrated. Fig.9 compares the two images captured under the normal and the dynamic range boosting modes, and the saturated area inside the light bulb can be clearly viewed in the dynamic range boosting mode.

4. Conclusion

A new efficient and simple CIS readout architecture providing both variable-resolution imaging and dynamic range boosting modes is successfully demonstrated in this paper. It requires minimal changes in pixel placing and routing and allows for a better aperture ratio. The proposed method provides a real-time,

simplified and accurate variable-resolution imaging, which can accelerate data processing speed, and reduce image processing complexity.

Acknowledgments

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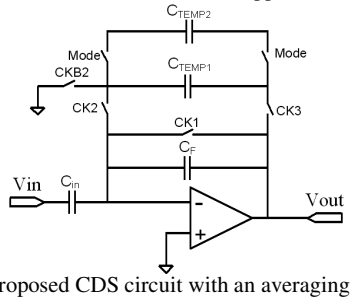


Fig.1 Proposed CDS circuit with an averaging mode

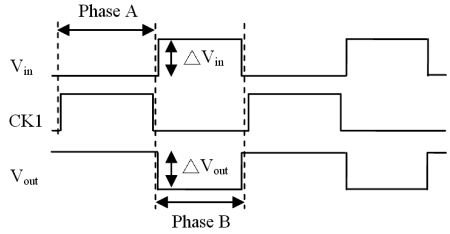


Fig.2 Timing diagram of the control signal of normal mode

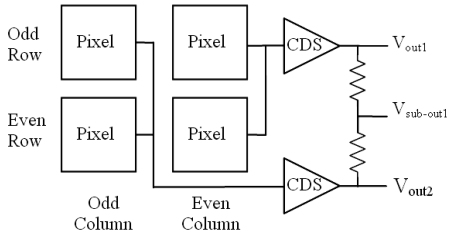


Fig.3 The averaging circuit schematics

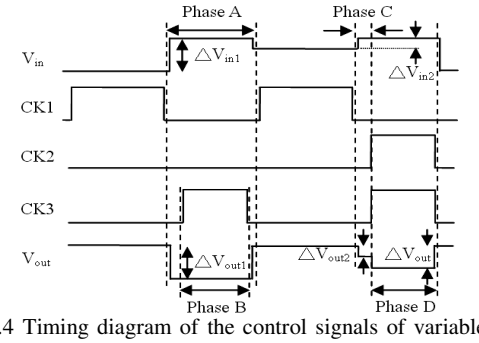


Fig.4 Timing diagram of the control signals of variable resolution mode

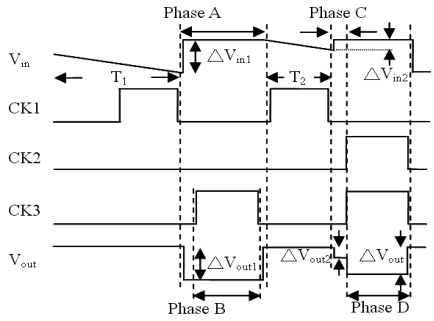
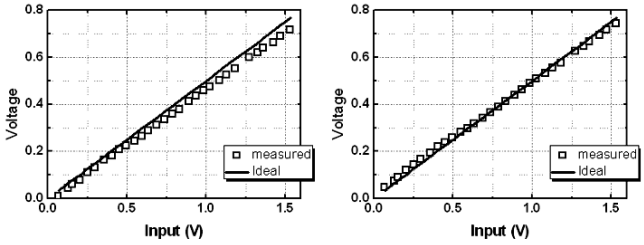
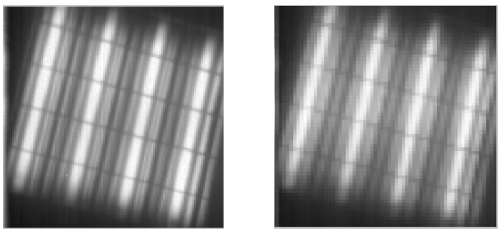


Fig.5 Timing diagram of the control signals of dynamic range boosting mode



(a) CDS averaging (b) Resistances averaging

Fig.6 The averaging outputs of CDS and resistor circuits respectively



(a) Normal mode (b) Low resolution mode

Fig.7 Captured images under two different modes

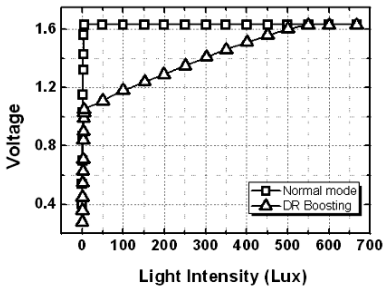
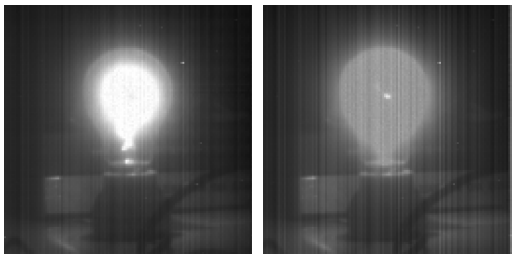


Fig.8 Optical response of a pixel under normal and DR boosting modes



(a) Normal mode (b) DR boosting mode

Fig.9 Captured images under two different modes