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High Sensitivity Dynamic Range Enhanced CMOS Imager with Noise Suppression

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1. Abstract

A high sensitivity CMOS image sensor solving the trade off between sensitivity and dynamic range has been developed by implementing a small capacitance high conversion gain floating diffusion (FD) in conjunction with a lateral overflow capacitor (CS) in a pixel. The noise floor is found to be suppressed in accordance with the noise factor theory. Two concerns, the degradation of S/N ratio (SNR) at a switching point from low light signal (S1) to bright light signal (S2) and the leakage at FD are solved by the optimum design of the CS capacitance and lower electrical field FD formation. A 1/4-inch VGA ($640^H \times 480^V$) 5.6×5.6-μm^2 pixel CMOS image sensor with the high sensitivity pixel approach has been fabricated through 0.18-μm 2P3M technology. The image sensing performance results in 200-μV/e$^-$ conversion gain, 2.2-e$^-$rms noise and 100-ke$^-$ full well capacity. The SNR degradation at S1/S2 switching points is invisible in the sample image.

2. Introduction

High sensitivity image sensing keeping or extending a dynamic range is strongly required for security camera application, especially capturing its best suit scene like one object under bright light and the other object in darkness. One of the approaches to realize the high sensitivity image sensing is to use a small floating diffusion (FD) capacitance, achieve a high conversion gain (Gc) and reduce input equivalent noise of image sensors [1]. However, the conventional small FD approach is well known to lose full well capacity and lead to degradation of the dynamic range. In order to solve the trade-off between the full well capacity and the high sensitivity, the new pixel circuit with a FD connected to a lateral overflow capacitor (CS) through a switching transistor has been proposed [2]. Low and bright light signal charges are converted to voltages (S1 and S2) via the small FD and the FD+CS capacitors respectively. The signal switch from S1 to S2 is performed when S1 signal is close to saturation. These two signals include different input equivalent noise floor at S1/S2 switching, however no theoretical analysis of the S/N ratio (SNR) delta between S1 and S2 has been discussed yet. In addition, S2 should have relatively small charges at S1/S2 switching point because the new high sensitivity approach has the limited well capacity at FD. Tolerance for FD dark current shot noise which is not issue in the previous wide dynamic range approach [3] is a possible concern in the high sensitivity approach even if the same pixel circuit is used. This paper describes the theory of the optimum CS capacitance design for the high Gc FD approach, high tolerance for the SNR degradation at S1/S2 switching point and low leakage FD formation with the low electrical field p-n junction.

3. Conceptual Advantage of High Sensitivity Approach

In order to achieve a high sensitivity keeping a high SNR, it is important to amplify the signal at earlier stage of the readout circuit. The first stage amplification is conceptually the best approach to suppress noises generated at respective circuit blocks from photo-detection node to device output buffer. The typical readout circuit of the CMOS image sensor consists of a FD to convert photo-electrons to the signal voltage, a pixel source follower, two pairs of signal and noise hold circuits for the reset noise subtraction and output buffers as shown in Fig.1. The total readout circuit noise factor, which is defined as the SNR of the input signal divided by SNR of the output signal, is described by the formula inserted in the figure [4]. This formula shows that the high Gc at the FD which corresponds to the 1st stage gain reduces the input equivalent noise of the subsequent circuit block. Fig.2 explains the concept of the high sensitivity CMOS image sensor in contrast with the conventional high sensitivity approach with the small FD causing the poor full well capacity and dynamic range. On the other hand, the pixel circuit in Fig.1 converts overflowed charges from the FD at the FD+CS capacitors. Both the FD and CS capacitances are the most important parameters for the high sensitivity pixel circuit design because the signal S1 whose kTC noise is eliminated by the noise subtraction achieves higher Gc, which is G_1 in Fig.1, compared to the signal S2 including inter-frame kTC noise [3]. The input equivalent noise floor difference between S1 and S2 leads to the SNR degradation at the S1/S2 switching point as shown in Fig.3.

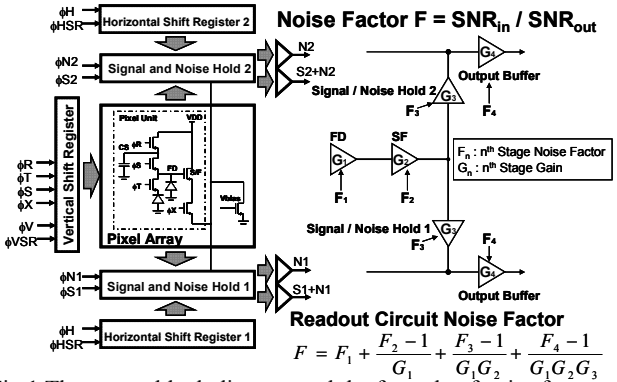

Fig.1 The sensor block diagram and the formula of noise factor.

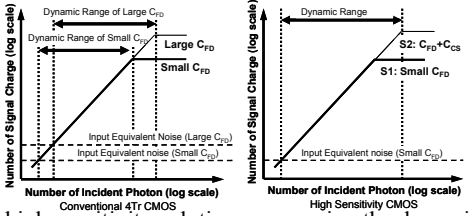

Fig.2 The high sensitivity solution overcoming the dynamic range trade-off compared with the conventional approach.

The white 100% level signal needs to be reproduced by S2 signal since the FD well capacity of the high sensitivity CMOS image sensor is not enough to keep even a usual dynamic range. The SNR of S1 is described by using the number of the signal charges expressed as N and the read-out circuit input equivalent noise expressed as NF.

$$S/N = \frac{N}{\sqrt{N + NF^2}} \qquad (1)$$

On the other hand, the SNR of S2 described as follows is lower than that of S1 because of the poor input equivalent noise which caused by relatively low Gc at the FD+CS in addition to the inter-frame kTC noise.

$$S/N = \frac{N}{\sqrt{N + (NF \cdot \beta)^2 + 2kT(C_{FD} + C_{CS})/q^2}} = \frac{N}{\sqrt{N + (NF \cdot \beta)^2 + 2kT(\frac{\beta}{q \cdot G_C})}} \qquad (2)$$

Parameter β which is defined as $(C_{FD}+C_{CS})/C_{FD}$ means the Gc ratio of S1 to S2. T, q and k are temperature in Kelvin, unit charge in coulomb and Boltzmann constant respectively. Fig.4 shows the SNR degradation at the S1/S2 switching point dependency on the number of signal charges as a parameter of β and Gc. The high Gc FD not only reduces the readout noise but also improves the SNR degradation at S1/S2 switching point. It means that the small FD capacitance realizes the S1/S2 signal switching at small number of charges without decrease of the dynamic range compared to the combination of CS and nominal capacitance FD. This result implies the smaller CS capacitance, which decreases proportionally to the FD capacitance, reduces input equivalent noise and offsets the small number of charges at the S1/S2 switching point. Another advantage of the CS capacitor integrated in the pixel circuit is high tolerance for the dark current in the signal S2 [3]. Since the signal S2 is a mixture of the non-saturated and the saturated overflow charges, S2 at least contains the S1 saturated charges. In addition, the high sensitivity concept is ideal for the reduction of S2 dark current because the electrical field reduction between N-type floating diffusion and P-well is effective for both the small FD capacitance and the low p-n junction leakage.

4. Device Fabrication and Image Sensing Performance

A 1/4-inch VGA color high sensitivity CMOS image sensor has been fabricated through 0.18-µm 2P3M technology to confirm high tolerance for SNR degradation at the S1/S2 switching point, dynamic range enhancement with low noise floor and high full well capacity and low S2 dark current shot noise at the S1/S2 switching point as shown in Fig.5. The lower electrical field at FD using the optimum P-well ion implantation has been taken to reduce the dark current shot noise included in S2 signal. Table I summarizes the image sensing performance. 200-µV/e$^-$ Gc at FD with the suppressed SNR degradation of S2 at 3000 electrons is achieved and the dynamic range is enhanced to 93-dB. Fig.6 is sample images reproduced by S1/S2 signals. High tolerance of the S2 dark current is found and it leads to the superior image quality with no significant visible noise due to the small FD dark current.

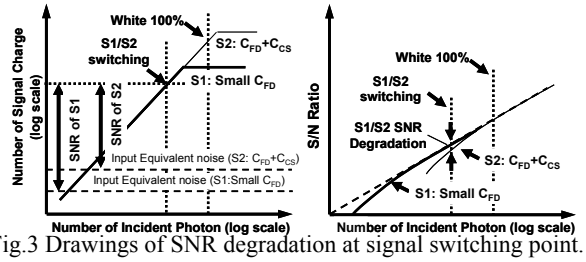

Fig.3 Drawings of SNR degradation at signal switching point.

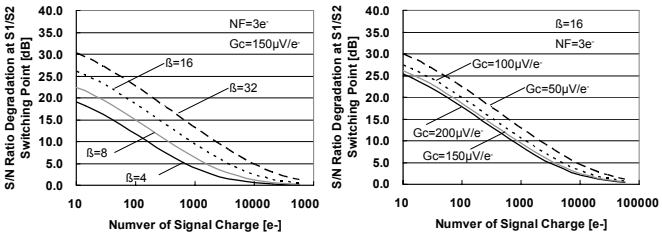

Fig.4 SNR degradation simulation at signal switching point.

Table I Measured performance of VGA chip.

Process Technology	0.18-µm 2P3M CMOS
Optical Format	1/4-inch VGA (5.6µm pixel, RGB Bayer CF)
Conversion Gain at FD	200-µV/e$^-$
S1 Noise Floor	2.2e$^-$
S1 Full Well Capacity	7000e$^-$
ß=$(C_{FD}+C_{CS})/C_{FD}$	10
SNR Discontinuity at 30FPS	3.3-dB at 3000e$^-$ 2.4-dB at 6000e$^-$
S2 Full Well Capacity	100-ke$^-$
Dynamic Range	93-dB

Fig.5 Chip micrograph.

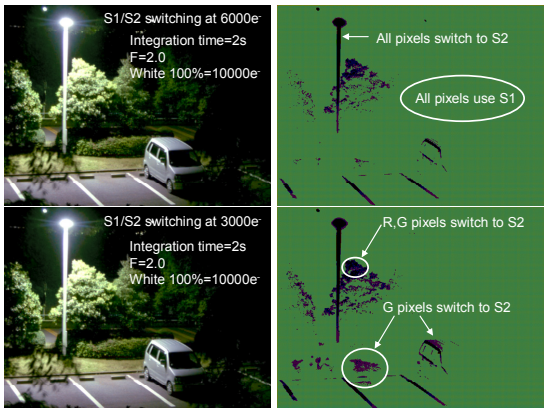

Fig.6 Sample images and S1/S2 signal selection map.

5. Conclusion

The high sensitivity CMOS imager solving the trade-off between sensitivity and dynamic range has been developed by implementing a small capacitance floating diffusion (FD) in conjunction with a lateral overflow capacitor (CS) in a pixel. The 1/4-inch VGA ($640^H \times 480^V$) 5.6×5.6-µm^2 pixel CMOS image sensor demonstrates the high conversion gain (200-µV/e$^-$), the low noise floor (2.2-e$^-$rms) as theoretically anticipated from the noise factor equation, the sufficient full well capacity (100-ke$^-$), the improved SNR drop at S1/S2 switching point and the low FD leakage.

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