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Embedded Process and Characterization Analysis of Discrete

H-1-6

Capacitor in Organic-Base Substrate

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Abstract

One of serious issues of advance packages on radio frequency application is simultaneous switch noise (SSN). In this study, a novel integration process of capacitor embedded in organic substrate is presented, and the effect of reducing switching noise with and without discrete capacitor will be shows by simulation and measurement.

1. Introduction

The fast improvement of wireless communication today, demand for more light, thin, and small electronic product that can bring anywhere. That's mean the design of the substrate to place a maximum number of passives is more complex. Capacitor played a major role to reduce simultaneous switching noise, SSN, in power deliver system of package. In this study, 0402 100nF capacitor is embedded in organic package substrate, dimension of substrate structure is as shown in figure 1. By embedding the capacitor in to the build up substrate has potential to get high electrical performance, area and cost saving, also improve the reliability of the solder mount. The electrical performances are measured by Vector Network analysis with high frequency probing system up to 3 GHz, and simulation of the substrate structure using Ansoft HFSS.

2. Embedded Process Flow

Embedding discrete capacitor in organic package substrate to reduce SSN and compatible with traditional substrate process, we provide one advance fabrication flow in figure 2. In this flow, 450µm core layer of substrate material is baked first, and then perform core layer pattern by electroplating. At traditional process flow, all of core via is perform by plating through hole (PTH). Connect 0402 capacitor and core copper layer by laser via is process characterization in this study. We put 0402 capacitor in core material, laser via drilling, and then up and down layers are laminated to perform complete substrate. Finally, all of the I/O pads are perform, solder-masker and Ni/Au plating steps are placed to prevent copper layer and I/O pads from oxidation. -182-

3. Experiment

In this work, different kinds of test fixture are fabricated by embedded process flow, with and without discrete capacitor embedded. And all of these test fixtures are simulated using Ansoft HFSS and Agilent ADS. 2-port S-parameters were measured by Agilent 8722ES Vector Network Analyzer with Cascade RF probes and RF1 probe-station from 10MHz to 3GHz, a standard SOLT calibrate were done to remove errors items caused by the measurement system.

4. Results and Discussion

Failure analysis process is used to inspect via connect performance between discrete capacitor and core layers, figure 3 shows SEM picture of this cross-section, that shows the connect performance is very well.

Main purpose of capacitor is to reduce switching noise, figure 4 shows the main structure of test fixture we used in this study. In this structure, two test point in one plane is designed to measure frequency response performance, with and without decoupling capacitor embedded in it, and to simulate by Ansoft HFSS. Measurement and simulation results are shown in figure 5 without capacitor and figure 6 with capacitor. The measurement result comparison is showed in figure 7. By this results, we see that the better insertion loss (S_{21}) bandwidth of capacitor embedded in substrate than substrate didn't capacitor embedded in it. That is to say that better high speed and high frequency performance will be expected when capacitor embedded in substrate by this process.

5. Conclusions

In this paper, we present one integrated fabrication process of embedded discrete capacitor in organic substrate, and capacitor and copper plane connect performance is checked. Measurement and simulation of embedded capacitor in the substrate is presented in this paper. Capacitor embedded in substrate will save total area of passive components in substrate, improve design freedom of IC package architecture, and further the effective of power integrity solution.

References

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Figure 1: Cross-section and dimension of finished embedded capacitor.





Figure 3: SEM picture of substrate cross-section.



Figure 4: Embedded capacitor substrate 3D model.



Figure 5: Measurement and Simulation data of substrate without 0402 capacitor.



Figure 6: Measure and simulation of substrate with embedded 0402 capacitor.



Figure 7: Comparison of substrate with and without 0402 capacitor.