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Silicon Nanowire Schottky Barrier NMOS Transistors

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1. INTRODUCTION

Erbium (Er) silicide has drawn considerable technological interest recently as a potential candidate to fabricate Schottky barrier NMOS due to its low barriers height ~0.3 eV to electrons [1]. However, the reported current drive ~300 μA/μm [4] is low. Nanowire transistors [3], due to enhanced drive currents and better control of channel potential, when fabricated with Schottky barrier source/drain, could be the one of the important structures for future device scaling. While Schottky S/D FinFETs have been demonstrated [8, 11-12], Schottky S/D nanowires with much smaller dimensions (~8nm) are reported in this work.

The devices shows Schottky barrier transistor behaviour with high I_{on}/I_{off} ratio ~ 10^5, high drive current ~1200μA/μm. This value is significantly higher than previously reported Schottky Barrier MOSFETs without barrier modified junctions[13]. Barrier height modification is also observed which is believed to be caused by the effect of trapped oxide charges on the reduced geometry of the Er-silicide/nanowire junction.

2. EXPERIMENTAL

Fig. 1 shows the process flow of transistor fabrication which has also been described in Ref. [3] up to the top nanowire removal by dry etching. This leaves the bottom nanowire as shown in Fig. 2a. The top nanowire removal was followed by SiN dummy gate deposition, patterning and etching. The SiN dummy gate (Fig. 2b) serves to isolate the source and drain during silicidation process. Erbium was sputter deposited using a PVD system followed by Rapid thermal annealing (RTA). The non-reacted Er was removed using a sulphuric peroxide mixture (H_2SO_4:H_2O_2~1:1). The silicide thickness was checked using TEM on the S/D pads as shown in Fig. 2c. The nanowire is triangular in shape with a base of 8nm as shown in Fig. 2d. It must be noted that there is no doping and subsequent thermal activation which greatly reduced the number of processing steps.

3. RESULTS

Fig. 3 shows the measured sheet resistance, R_s values of ~85nm thick $ErSi_{2-x}$ plotted with the required R_s as specifed by the International Technology Roadmap for Semiconductors [2]. As device scaling proceeds toward sub 22nm technological node, the sheet resistance of the $ErSi_{2-x}$ Schottky S/D architecture remains constant at 10 Ω/sq.

Fig. 4 shows the *I-V* characteristics of a planar erbium silicided schottky diode. The curve shows near ideal metal/*p*-Si contact (ideality factor ~1.07). The measured barrier height to holes, Φ_{peff} is 0.79eV and the junction leakage current measured is 8.95fA/μm^2 which are comparable/better than most reported values [4].

Fig. 5 shows the back gated I_d-V_g characteristics of the erbium silicide SiNW NMOS with a single 350 nm long nanowire as the channel. The device shows high drive current (1200μA/μm) in positive gate voltage direction. The I_{on}/I_{off} ratio is ~10^5. The measured SS is 120mV/dec which is better than the reported SS for back gated SiNW transistors of 300mV/dec [5] and 174mV/dec [6]. Shown in Fig. 6 is the I_d-V_d plots of the same device.

Fig. 7 shows the I_{on}/I_{off} characteristics of the fabricated SiNW transistors compared to various devices found in literature [3, 7-12]. The fabricated SiNW transistors show higher drive current than planar bulk/SOI Schottky Transistors and are comparable with multiple gated Schottky FinFETs.

Fig. 8 shows the peak transconductance, gm of the fabricated SiNW transistors with a single SiNW channel (control) vs. side by side (2 wire) SiNW channels against the channel length from 200 – 1000nm. The transconductance is higher for 2 wire channels.

Fig. 9 shows the comparison of drive current of the fabricated SiNW transistors against the channel length from 200 – 1000nm. Side by side (2 wire) SiNW transistors show higher drive current compared to control SiNW transistors in agreement with the transconductance results. This indicates that device performance can be boosted by increasing the number of wires. 'Larger' SiN dummy gate and 'Thinner' silicide SiNW transistors showed lower drive currents compared to control SiNW transistors. The reason is these variations directly impact the physical structure of the transistors, (e.g. devices patterned with larger SiN dummy gate have Schottky junctions further from the SiNW channel) resulting in larger series resistance.

Fig. 10 shows the temperature dependent I_d-V_g curves of a particular Er-silicide SiNW transistor measured at V_d = 1.2V. The arrhenius plot (not shown here) extracted from Fig. 10 was used to extract activation energies for various V_g as shown in Fig. 11. This activation energy, E_a corresponds to the barrier height (both hole and electron), Φ_{eff} as V_g modulates the SiNW band profile. The inset shows the proposed conduction band diagram when the SiNW channel is 'ON' at positive V_g voltages.

As can be seen, channel inversion occurs at $V_g \geq 0$V where E_a = 0.32eV as this value is approximately equal to the value measured on the bulk diode (1.12 – 0.79eV = 0.33eV). Also from Fig 11, the maximum E_a occurs at a negative V_g value and is greater than the bulk diode value of 0.79eV. These 2 observations imply that the *n*-channel is already 'ON' at V_g = 0V possibly due to the presence of positive oxide trap states in the gate oxide which (a) lowers the electron barrier height and increases the hole barrier height due to the influence of a dipole layer at the metal/semiconductor interface [13] and, (b) induces negative charge in the SiNW channel even without the application of a gate voltage.

4. CONCLUSIONS

We have fabricated of erbium silicided Schottky barrier S/D NMOS transistors using silicon nanowires with reduced dimensions ~8nm as the channel. Devices showed good electrical characteristics in term of I_{on}, I_{off} and SS. Improvement in the device performance is shown by optimizing device physical structure and using multiple channels. Barrier height modification is also observed due to the effect of oxide trapped charges.

Acknowledgements
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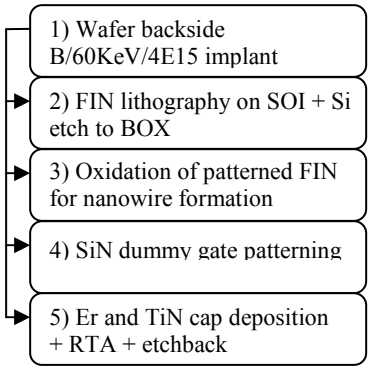

Fig.1 Process Flow.

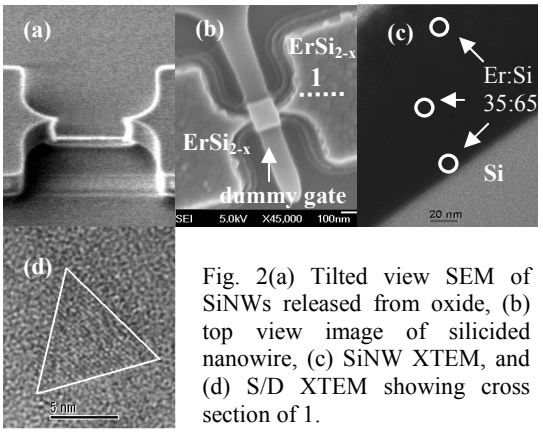

Fig. 2(a) Tilted view SEM of SiNWs released from oxide, (b) top view image of silicided nanowire, (c) SiNW XTEM, and (d) S/D XTEM showing cross section of 1.

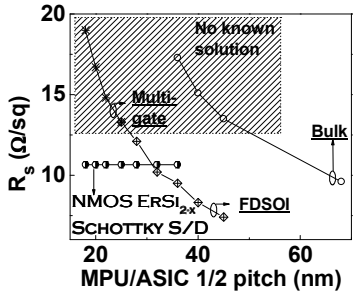

Fig. 3 R_s vs. MPU/ASIC ½ pitch for various MPU\ASIC design architectures.

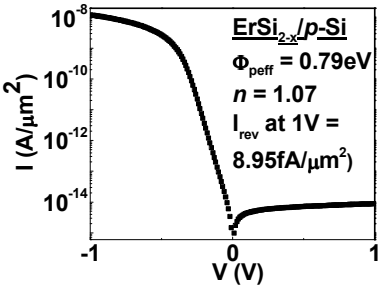

Fig. 4. *I-V* curve of a $ErSi_{2-x}$/*p*-Si(100) diode.

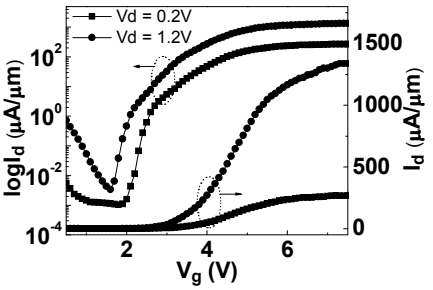

Fig. 5 I_d-V_g of a Er silicided SiNW transistor.

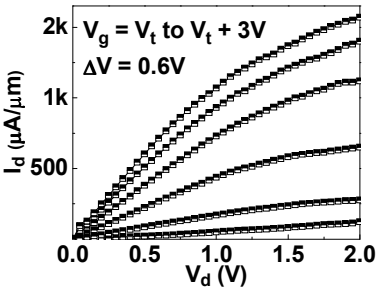

Fig. 6 I_d-V_d of a Er-Silicided SiNW transistor.

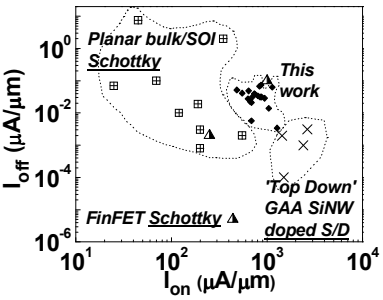

Fig. 7 Comparison of I_{on}/I_{off} characteristics of (silicided/SiNW) transistors. Refs. 3, 7-12.

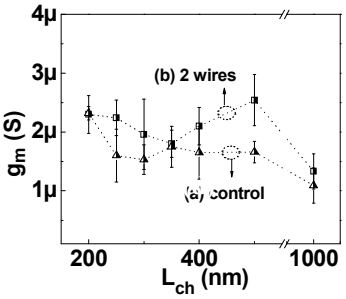

Fig. 8 Comparison of Er silicided SiNW transistors transconductance (a) control, and (b) side by side : 2 wires.

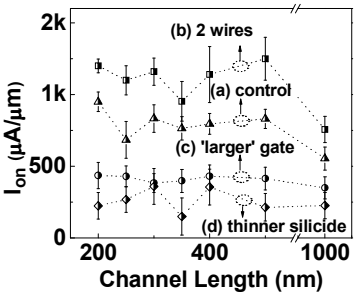

Fig. 9 Comparison of I_{dsat} for (a) control, (b) side by side, (c) 'larger' nitride dummy gate, and (d) thinner S/D silicide thickness

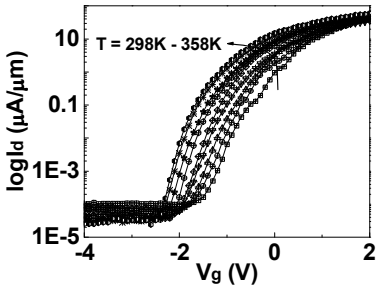

Fig. 10 (a)Temperature dependent I_d-V_g curves of an Er silicided SiNW transistor.

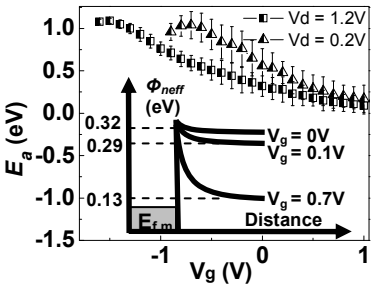

Fig. 11 Extracted E_a against V_g at different V_d. Error bars indicate fitting errors. Inset shows the conduction band profile in subthreshold region (V_g = 0, 0.1V) and ON state (V_g = 0.7V) upon SiNW channel inversion.