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Poly-Si Nanowire Thin-Film Transistors with Inverse-T Gate

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1. Introduction

Silicon nanowires (NWs) are attractive for a variety of applications, including nano CMOS [1], memory devices [2] and biosensors [3]. Recently, we proposed a novel technique to fabricate self-aligned poly-Si nanowire TFT (NW-TFT) featuring a very simple and low-cost process flow [4] [5]. Due to the inherent large surface-to-volume ratio of NW, strong gate control could be exerted, resulting in the suppression of undesirable short channel effects (SCEs). While NW channel is shown to be beneficial for enhancing the device performance in our previous work, the spacer-shape channel is manipulated by only a single side-gate. In this work, a unique and high-performance inverse-T gate (ITG) NW-TFT is fabricated and characterized. Moreover, by further adding a top gate, together with the inverse-T gate, much better gate controllability over NW channel is achieved, resulting in a higher ON-current, reduced short channel effects and steeper subthreshold slope (S.S.).

2. Device Fabrication

The fabrication process sequence is similar to that described in our previous work [5]. Schematic structure of the proposed inverse-T gate NWTFT is shown in Fig. 1. After depositing 150nm in-situ-doped n^+ poly-Si, the inverse-T gate was fabricated by twice applying a standard G-line lithography and dry etching processes. The inverse-T gate oxide was an 18.5nm-thick TEOS deposited by LPCVD. Two NW channels were formed self-aligning to the inverse-T gate simultaneously with source and drain (S/D) definition. The devices were then split into two groups, with top-gate (denote as ITDG) and without top-gate (denote as ITG) above the NW channels. LPCVD TEOS with thickness of 18.5nm was deposited to serve as top-gate oxide. 100nm in-situ-doped n^+ poly-Si was deposited and patterned to serve as the top-gate electrode. All devices were then covered with 200nm TEOS as passivation layer. All fabricated devices received a 3-hour plasma treatment in NH_3 ambient.

3. Results and Discussion

The cross-sectional TEM image of a NW channel is shown in Fig. 1 (b). The dimensions of the triangular NW channel cross-section are 40nm, 50nm and 80nm. Fig. 2 shows transfer and output characteristics of ITG and ITDG NWTFTs, respectively. Because of larger conducting area and better gate-controllability, the ITDG device apparently has higher ON current and steeper S.S. (128mv/dec versus 150mv/dec). Note that SCEs in both devices are essentially eliminated. In Fig. 3, the current ratio of ITDG to ITG devices becomes lower by increasing the V_G - V_{TH}. The error bars represent the current ratio variances by varying drain voltage through 0.1V to V_G - V_{TH}. It could be explained that, with increasing V_G, the NW channel surface conducting area of the ITG device is enlarged by gate fringing field and corner effect of the NW channel. But for ITDG device, its NW channel is surrounded by inverse-T gate and top gate, so no extra area could be induced.

Fig. 4 depicts transfer characteristics of the ITDG NWTFT by sweeping one gate, while varying the remaining gate voltage from 2V to -3V. The curves were all normalized by subtracting OFF-current. Owing to the small volume of NW, the channel potential is sensitive to both gates, and strong gate-to-gate coupling phenomenon is observed. Fig. 4 also reveals that the controllability of the inverse-T gate is better than that of the top gate. It might be because of the wider channel width and relatively thinner channel thickness under the control of inverse-T gate. According to the back-gate-effect [6], the drive gate has to overcome the impact of the back-gate on NW channel potential. So that the subthreshold slope of ITDG device, when driven by inverse-T gate, is reasonably larger than that of device without top-gate (ITG) (Fig. 4(a)). In addition, the S.S. and ΔV_{TH} both become smaller when the top gate bias is lower than the V_{TH} of ITDG mode (V_{THDG}). By introducing the back-gate-effect factor $\gamma = dV_{TH(ITG)}/dV_{TG}$, which is smaller when $V_{TG} < V_{THDG}$ ($\gamma = 3T_{OX(ITG)}/(3T_{OX(TG)}+T_{Si})$) and larger when $V_{TG} > V_{THDG}$ ($\gamma = (3T_{OX(ITG)}+T_{Si})/3T_{OX(TG)}$) [6], this phenomenon can also be well understood.

4. Conclusions

In this work, a novel high-performance inverse-T gate NWTFTs were fabricated and characterized. Enhanced performance under the ITDG mode has been demonstrated, including higher ON current, larger ON/OFF ratio and sharper S.S. reaching 128mv/dec. Moreover, since the dimension of the NW channel is small enough to cause strong coupling between the inverse-T gate and the top gate, the gate-to-gate coupling effect in ultra-thin body device can be studied by utilizing the proposed double-gated structure.

Acknowledgments

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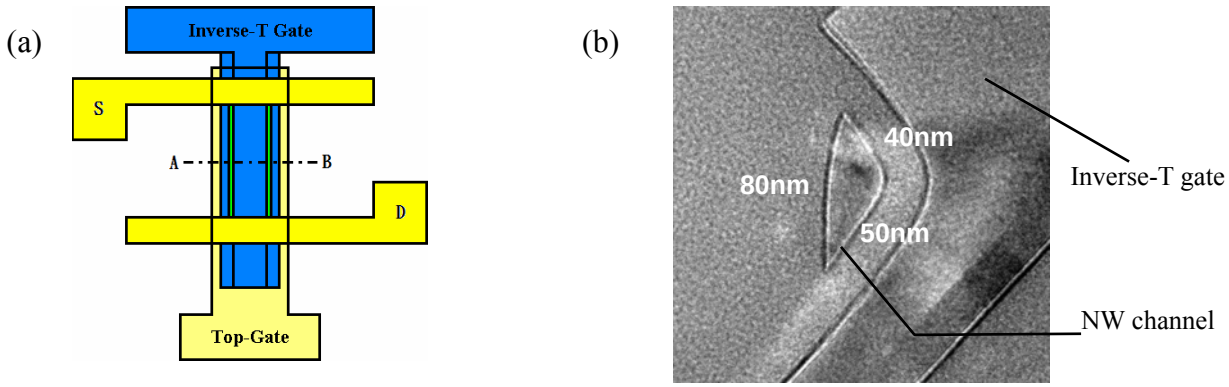

Fig. 1 (a) Top view of the NW-TFT with inverse-T gate and top gate structure, (b) cross-sectional TEM of ITG NWTFT.

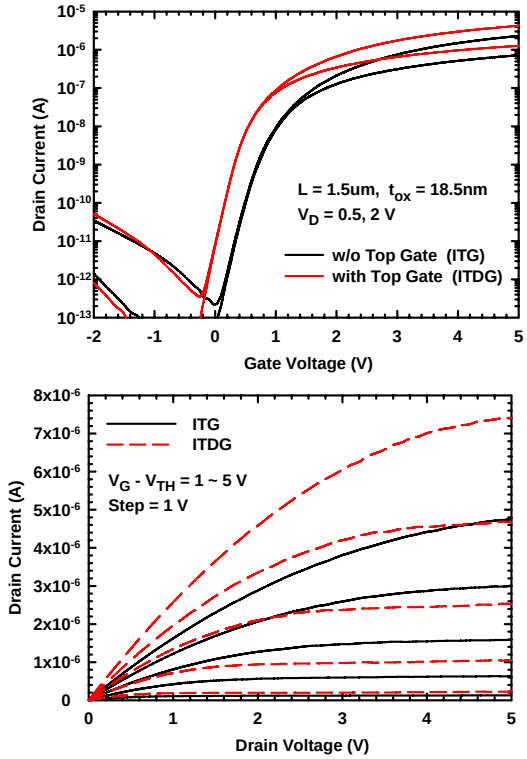

Fig. 2 Transfer and output characteristics of ITG and ITDG NWTFTs.

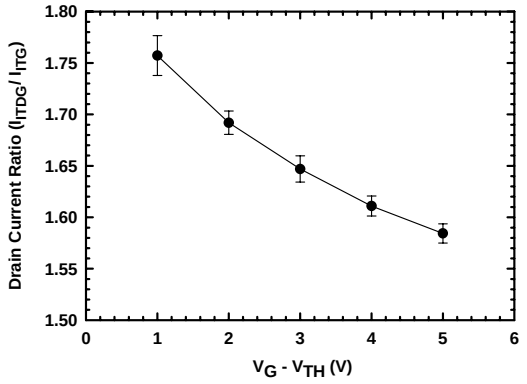

Fig. 3 Current ratio of ITDG device to ITG device at different $V_G - V_{TH}$ values.

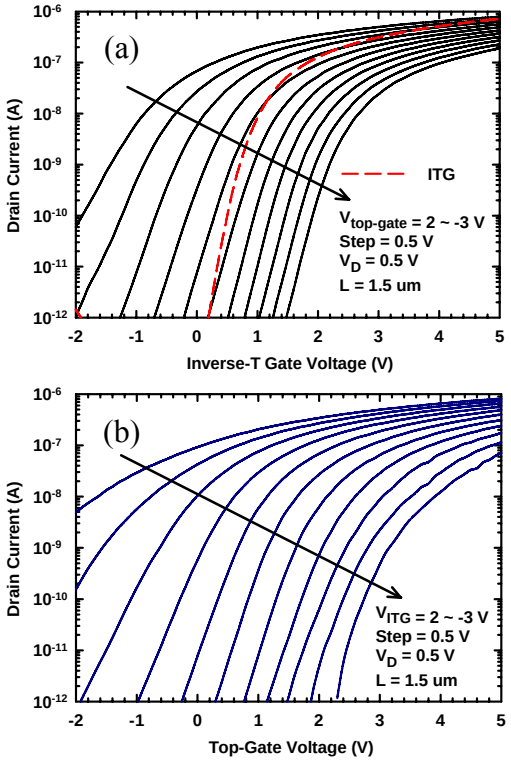

Fig. 4 I_d-V_g characteristics of the ITDG NWTFT by sweeping (a) inverse-T gate and (b) top-gate biases (modified).

	SS (mV/dec)	I_{on} (μA)
ITG	150	0.66
ITDG	128	1.07
Top-gate = -1V	215	0.40
Top-gate = 0V	250	0.44
Top-gate = 1V	290	0.45

Table 1. Performance parameters for NWTFTs with different gate-control modes. (V_D = 0.5V, I_{ON} @ V_G-V_{TH} = 4V)