H-6-2

Strained Ge-rich SiGe Nanowire pFETs with High-κ/Metal Gate Fabricated using Germanium Condensation Technique

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1. Introduction

Multi-gate device architectures such as Fin-FET, Omega-gated FET and gate-all-around (GAA) FET have attracted much attention due to their better immunity to short channel effects (SCE) and large improvement of drive current [1]-[5]. In such fully-depleted devices, the gate electrostatic control is further enhanced with shrinking of channel body dimension, which makes the multi-gate nanowire transistor architecture extremely attractive. The ultimate shrinking of the channel dimension leads to nanowire devices. Two approaches have been developed for nanowire fabrication. A bottom-up method, such as VLS, has been used for Si/SiGe nanowire fabrication but has less potential for integration [4]. By using lithography and controlled oxidation, a top-down approach for nanowire fabrication can be manufacturable due to its compatibility with CMOS processes. GAA Si-nanowire transistors have been successfully fabricated [5]. The devices showed excellent performance and better control over short channel effects. Being a high mobility material, Ge-nanowire devices are expected to perform even better. High mobility in grown Ge-nanowires has been demonstrated [6]. However, Ge/Ge-rich-SiGe nanowire transistors, fabricated using top-down approach, have yet to be demonstrated.

In this work, we report the first demonstration of Ge-rich (58%), ~13nm thick SiGe nanowire p-FET with HfO_2 gate dielectric and TaN Omega gate fabricated using a top-down approach. A two-dimensional Ge condensation technique was used to obtain Ge-rich strained nanowire channels connected to Si-rich S/D pads. The nanowire devices show excellent DC performance demonstrated by low V_{TH}, large I_{ON}/I_{OFF} ratio ~10^5, low DIBL ~40mV/V and acceptable subthreshold swing ~160mV/dec.

2. Device Fabrication

The process flow for the fabrication of p-channel SiGe nanowire transistors with HfO_2/TaN gate stack is shown in **Fig. 1.** A (100) SOI wafer with a top Si-thickness (T_{Si}) of 70 nm was used. This was thinned down to 20 nm by thermal oxidation process. A 40nm thick $Si_{0.75}Ge_{0.25}$ was epitaxially deposited on the thin SOI substrate using UHVCVD. Oxidation and anneal cycles were used to one-dimensionally condense Ge into the top Si to produce an SGOI substrate [7]. This process cycles between 750°C to 950°C for 7 times. The lower temperature in the cycle helps to reduce defects and improve surface smoothness (RMS~0.33nm). Next, alternating phase-shift-mask lithography with a KrF scanner, plasma photoresist trimming and reactive ion etching were used to define SiGe fins down to 40-50nm in width. **Fig. 2(a)** shows the schematic after SiGe fin pattern transfer. **Fig. 2(b)** shows the cross-sectional schematics of the SiGe fin along the A-A' plane. After fin transfer, the wafer was oxidized at 875ºC for 15mins to two-dimensionally condense the Ge into the SiGe fin, bringing about size reduction as well as Ge enrichment. This second condensation process results in an oxide-encapsulated SiGe nanowire shown in **Fig.3(a). Fig.3(b)** shows the SEM image of an oxide-encapsulated SiGe nanowire before oxide removal. The SiGe nanowire is clearly observed, and is connected to S/D mesas with smooth surface morphology. After a selective wet etch of the oxide around the SiGe nanowire, the HfO_2/TaN gate-stack was deposited in a PVD system. After gate definition, the SiGe nanowire transistor fabrication was completed by S/D implantation, activation and metallization.

Fig. 4 shows the TEM image of the S/D area after condensation. It can be seen that the Ge concentration in the S/D area is ~30%. The Ge concentration varies only slightly from top to bottom, suggesting good uniformity in the SiGe layer after cyclic oxidation and annealing. **Fig. 5** is the cross-section TEM image of the SiGe nanowire with the HfO_2/TaN gate stack. The omega shaped gate structure can be seen clearly. EDX result shows that a Ge concentration of ~58 % was obtained in the SiGe nanowire, which has a diameter of ~13 nm. Three sides of the thin SiGe fin were exposed during the oxidation, allowing for two-dimensional Ge condensation. This result in higher Ge content in the nanowire thus formed, as compared to that in the S/D mesas (mainly one-dimensional condensation). The thickness of the HfO_2 is 8nm with a 60nm TaN layer on top.

3. Results and Discussion

The I_D-V_G characteristics of SiGe nanowire transistor with a gate length of 400 nm is shown in **Fig. 6**. The drain current was normalized by its diameter and the V_T was extracted to be ~0.125V. The subthreshold swing of this device is ~160 mV/dec. This can possibly be attributed to interface states at the gate dielectric interface, due to the absence of surface passivation prior to gate dielectric deposition. The SiGe nanowire device also shows good DIBL parameter of ~40 mV/V and a I_{on}-I_{off} ratio of 10^5. The I_D-V_D characteristics of the same device are shown in **Fig. 7**. The drive current at V_G-V_T = -1.0V is ~1000 μA/μm, which is exceptionally high for a long gate-length p-channel device. **Fig. 8** compares the transconductances at linear and saturation regions of a SiGe nanowire and a planar device which were fabricated on the same wafer. For clarity, the linear transconductance curve is shown in inset to the figure. The transconductance in both linear and saturation regions for SiGe nanowire devices are almost 22 times larger than planar devices. A minor portion (<2x) of this enhancement could have come from the thinner HfO_2 thicknesses on the nanowire sidewalls as a result of PVD deposition. However, a major portion (>11x) of this enhancement is likely to come from hole mobility enhancement as a result of uniaxial compressive stress and increased Ge concentration in nanowires (58% Ge in nanowire channels and 30% for planar). SiGe films formed using Ge condensation develop biaxial compressive stress as a result of increasing Ge content and limited viscous flow of the underlying buried oxide. Others have previously reported up to 10 times hole mobility enhancement due to this [7]. Shape anisotropy of the SiGe nanowire gives rise to anisotropic strain relaxation. In other words, strain perpendicular to the channel direction can be relaxed more easily than strain parallel to the channel direction, which makes the strain in the nanowire channel predominantly uniaxially compressive. **Fig. 9** plots the I_{on}-I_{off} ratio for L_G=400nm SiGe nanowire devices. This is the ratio of the drain current value at (V_G + 1.0 V) divided by that at V_G, as V_G moves from -1.5V to 1V. It can be seen that the I_{on}-I_{off} peak is >>10^4, suggesting good performance for such SiGe nanowire devices.

Fig.10 shows series resistance extraction using devices of different gate lengths biased in the linear region, estimating the absolute series resistance to be approximately ~10 kΩ. This corresponds to a value of 130 Ωμm if a nominal nanowire device width of 13 nm is assumed. **Fig.11** plots the peak of linear transconductance for different gate lengths. It can be seen that as the gate length decreases, the transconductance peak increases. **Fig. 12** compares the drive current for different gate lengths. The drive current shows the same trend as the transconductance peak. For this first demonstration, all the fabricated SiGe NW devices are long channel devices. It is expected that the performance of these devices will improve further when gate lengths are scaled down.

4. Conclusion

P-channel omega-gated SiGe nanowire FETs with high-κ/metal gate fabricated using a top-down approach was demonstrated for the first time. By using a two-dimensional Ge condensation technique, almost 60% Ge in the SiGe nanowire channel was achieved. The diameters of SiGe nanowires formed using this top-down approach are around 13nm. Excellent performance has been achieved with low DIBL, acceptable I_{on}-I_{off} ratio (10^5) and subthreshold swing. SiGe nanowire transistors greatly outperform their planar counterparts. Even better performance can be expected when the gate lengths are scaled down. With process optimization, this top-down approach can potentially allow for the integration of nearly pure Ge nanowire transistors into CMOS logic circuits.

References:

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- SOI thin down
- Epitaxy of SiGe layer on thin SOI substrate
- **SiGe layer 1st condensation (Cyclic oxidation and annealing to form SGOI substrate)**
- Fin definition (PR trimming produces narrow fins for NW formation)
- **Nanowire oxidation (2nd condensation)**
- Oxide release
- HfO_2/TaN gate-stack deposition
- Gate definition
- S/D implant and RTA activation
- PECVD SiO_2 deposition and metallization

Fig. 1 Process flow of SiGe nanowire P-channel FET with HfO_2/TaN gate stack using two-step Ge condensation technique

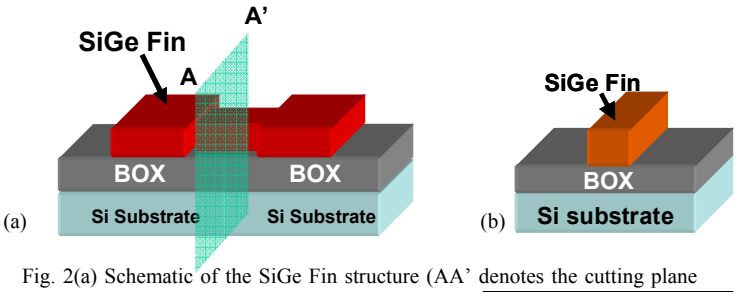

Fig. 2(a) Schematic of the SiGe Fin structure (AA' denotes the cutting plane of the fin.) (b) Cross-section schematic of SiGe Fin.

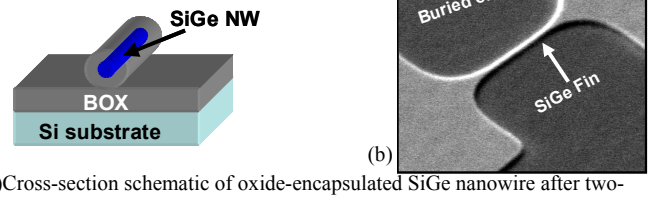

Fig. 3 (a)Cross-section schematic of oxide-encapsulated SiGe nanowire after two-dimensional Ge condensation. (b) SEM image of the SiGe fin after condensation

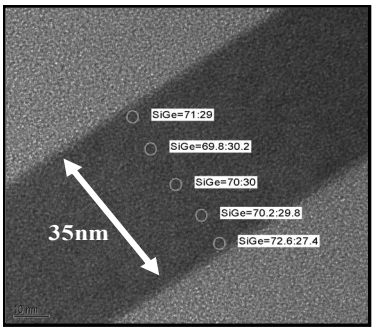

Fig. 4 TEM image of SiGe S/D area after condensation. Uniform Gee content concentration of 30 % was obtained

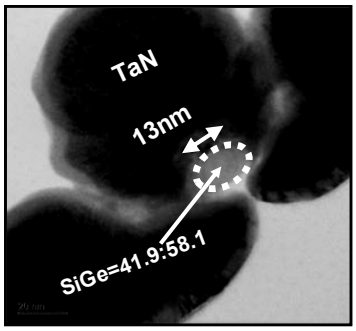

Fig.5 TEM image of SiGe nanowire (EDX shows Ge% ~58.1% , diameter is 13nm, 13nm, with 80A HfO_2 and 600A TaN)

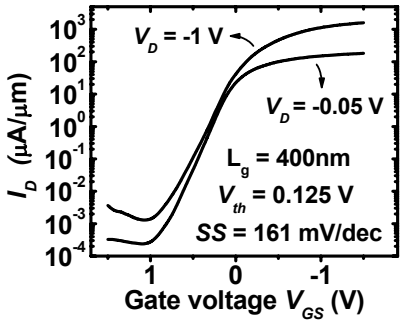

Fig.6 I_D-V_G characteristics of SiGe NW device with NW diameter of 13nm, L_g -400nm. DIBL ~ 40mV/dec, I_{on}-I_{off} ~ 10^5

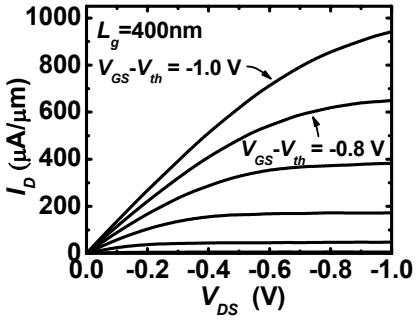

Fig. 7 I_D-V_D characteristics of the same device. Drive current is ~1000μA/μm @ V_G-V_T=-1.0V

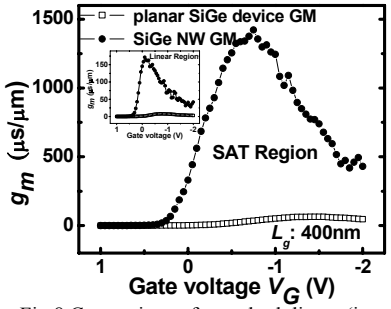

Fig.8 Comparison of g_m at both linear (inset) and saturation region between SiGe NW and planar SiGe devices. The SiGe NW with uniaxially compressive strain shows 22 times higher g_m than the planar device.

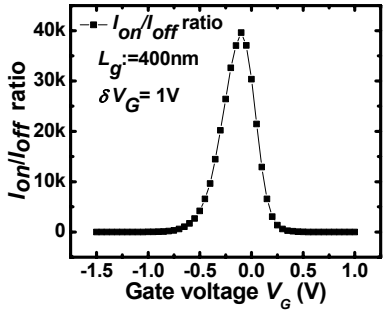

Fig.9 I_{on}-I_{off} ratio for 400nm SiGe NW. (I_{on}-I_{off} ratio = I_D value@V_G+1V divided by that @V_G. V_G from -1.5V to 1V)

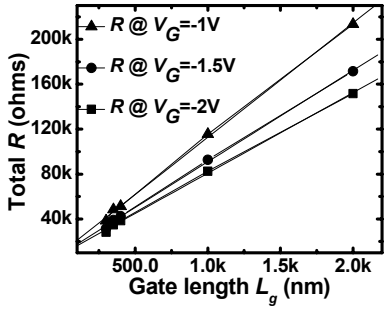

Fig.10 Plot of resistance as a function of L_g @ V_G =-1V,-1.5V,-2V. The extracted series resistance is ~10kΩ.

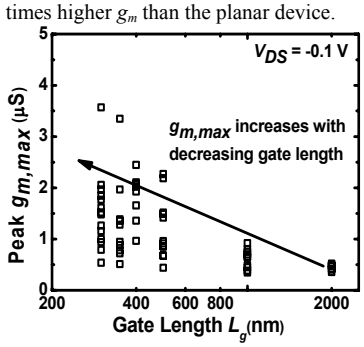

Fig.11 Plot of g_m peak as a function of L_g. As L_g decreases, g_m peak increases

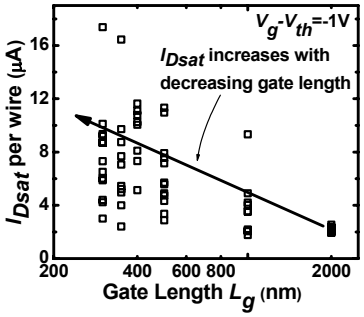

Fig.12 Plot of I_{Dsat} per wire versus L_g. I_{Dsat} performance improves when L_g decreases