Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 1074-1075

H-7-1 (Invited)

Jet-printed Polymer Transistor Display Backplanes

R. A. Street, A. C. Arias and J. H. Daniel

Palo Alto Research Center, 3333 Coyote Hill Road, Palo Alto, CA 94304

1. Introduction.

Printed thin film transistors (TFT) provide opportunities to reduce display manufacturing cost and enable roll-to-roll processing. Jet-printing in particular requires no physical mask, has digital control of ejection to provide drop-on-demand printing, and provides good layer-to-layer registration [1,2,3]. However, new materials and processing steps must be developed, since printing uses liquid materials, and there are many challenges in creating the technology. We describe recent progress towards jet-printed TFT backplanes, based on polymer solutions and nano-particle metal inks.

2. Materials and printing process

Nano-particle metals

Several solution-based materials are now available for the various layers of the TFT. The gate and source-drain contacts of our devices are made from nano-particle silver [3]. The advantages of this material are that it has sufficient conductivity for the data address lines, it can be jet-printed and the films sinter to a robust layer at low temperature compatible with deposition on plastic substrates, and silver forms a suitable contact to organic semiconductors [4]. The jet-printed Ag feature size depends on the surface energy of the substrate – a very hydrophobic surface causes the ink to break into droplets rather than forms continuous line, while a very hydrophilic surface gives undesirable spreading of the ink and very large features [5]. Figure 1 shows that on a suitable surface, the printed lines have straight edges and reasonable feature sizes.

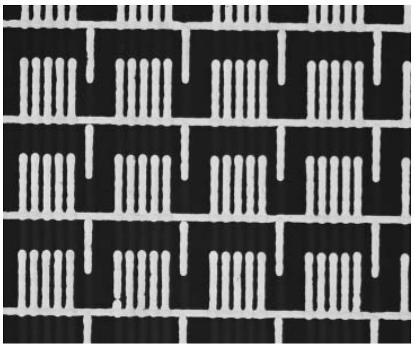

Figure 1. Photograph of a printed pattern using Ag nano-particle ink to form the gate layer of the array.

Figure 2 shows that the surface profile of the printed metal line is reasonably flat. The tendency for the nano-particle solute to migrate to the edge of a drying drop – the well-known coffee stain effect – can be controlled by suitable choice of the solvents.

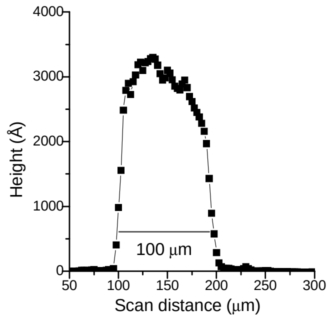

Figure 2. Profile of a printed Ag line with average thickness of 300 nm.

Polymer semiconductor and gate dielectric

The gate dielectric must combine good dielectric properties for the TFT with a suitable surface energy for the printed contacts and be chemically resistive to the layers placed on top. We have found that both PVP and SU-8 are suitable dielectric materials for our semiconductor [6]. The gate dielectric is spin-coated rather than jet-printed because it is a continuous layer in the TFT array.

The semiconductor is a polythiophene, PQT-12, which exhibits mobility ~0.1 cm^2/Vs on optimized surfaces [7]. One of the challenges of the printed TFT backplanes is to achieve similar mobility on the printed surface, with a polymer dielectric.

Printing processes

A piezo-electric jet-printing system is used to deposit the metal and semiconductor layers [8,9]. The printer uses a computer vision system to register the different layers, giving a ~5 micron position accuracy. The various print-heads used have nozzle size of 30-50 micron, and result in printed features sizes of 60-80 micron. The channel length between source and drain contacts can be made smaller than the feature size, because of the high printing accuracy.

Printed backplanes are made on both glass and 8 mil polyethylene napthalate (PEN). The PEN substrate is coated with a buffer layer to planarize and provide a suitable printing surface. The nano-particle silver is sintered at 150C after the solvent has dried, and the PQT-12 polymer is annealed at 120C to achieve high mobility.

3. Backplane fabrication and performance

The TFT is a bottom gate, bottom contact device with the structure illustrated in Figure 3.

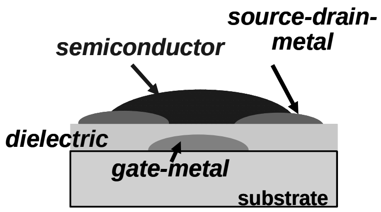

Figure 3. Schematic illustration of the bottom gate, bottom contact, printed TFT structure.

The backplane is intended for a active matrix reflective display. The pixel contains the TFT, gate and data address lines, the media contact pad and a pixel capacitance to minimize the feed-through voltage. The pixel size is 680x680 micron, which is largely determined by the feature size that we are able to print. The process involves three jet-printing steps and the spin-coated dielectric. Encapsulation of the TFTs can be done by spin-coating and we have shown that PMMA is effective.

We have fabricated small (2” diagonal) test array with a 50x50 pixel format using the process described above [5,6]. Figure 4 shows a photograph of the backplane and the pixel.

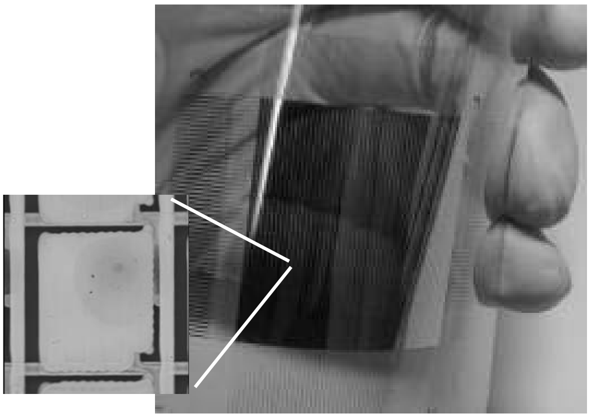

Figure 4. Photograph of the printed TFT backplane on PEN substrate, and an individual pixel.

The jet-printed TFTs have reasonable performance, and examples of the transfer characteristics in the saturation regime are shown in Figure 5. The typical mobility is 0.04 cm^2/Vs, and in a few cases mobility of ~0.1 cm^2/Vs was observed, which is the same as optimized lithographically patterned devices. The effective mobility is reduced by several mechanisms, including roughness of the dielectric, insufficiently hydrophobic dielectric surface and high contact resistance. It is therefore important to carefully optimize the materials and printing process to obtain high TFT mobility.

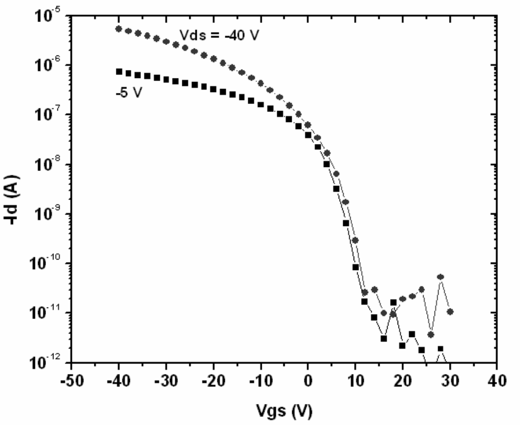

Figure 5. Transfer characteristics of a TFT using the printing process and on a PEN substrate.

4. Discussion and conclusions

We have demonstrated that a polymer TFT array can be jet-printed on a plastic substrate with reasonable TFT performance. The technology may be useful for e-paper, signage and other flexible electronics applications. Application to higher resolution and video rate displays is limited by the low mobility of the solution-based semiconductor and the large printed feature size. In the future both higher performance semiconductor materials and smaller jet-printer drop size can be expected.

Acknowledgements

We are grateful to B. Krusor and S. E. Ready for technical assistance, to B. Ong for providing the PQT-12 polymer semiconductor, to DuPont-Teijin for providing PEN substrates, to Cabot for supplying nano-particle Ag ink, and to the NIST Advanced Technology Program, contract 70NANB3H3029, for partial funding.

References

[1] B.-J. de Gans, P. C. Duineveld, and U. S. Schubert, Advanced Materials 16, 203 (2004).

[2] M. L. Chabinyc and A. Salleo, Chem. Mater. 16, 4509, 2004.

[3] A. C. Arias, et al., Appl. Phys. Lett. 85 (15), 3304 (2004).

[4] J. R. Greer and R. A. Street, Acta Metallica in press

[5] A. C. Arias, et al., JSID, in press.

[6] J. Daniel et al., Jap. J. Appl. Phys., 46, 1363, 2007.

[7] B. Ong et al., J. Am Chem Soc., 126, 3378, 2004.

[8] S. E. Ready et al., Proc. IS&T NIP, 18, 429, 2002.

[9] A. C. Arias et al., Appl. Phys. Lett., 85, 2070, 2003.