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An Analytic Current-Voltage Equation for Top-contact OTFTs Including the Effects of Variable Series Resistance

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1. Introduction

Recently, organic semiconductors are used not only to fabricate a single transistor but also to make integrated circuits such as RF ID tags. As a result, it is necessary to establish a physically meaningful device model to extend the applicability of organic thin film transistors(OTFTs). There have been experimental evidences[1] that the series resistance(R_{sd}) of OTFTs is dependent on the gate voltage(V_G), however, there has been no I-V equations which reflect this observation except a few empirical models[2]. In this paper, by analyzing the gate-source overlap region, an analytic I-V equation including the effects of V_G-dependent R_{sd} is derived and the equation is applied to the fabricated OTFTs.

2. Derivation of I-V equation

The cross section of a top-contact OTFT is shown in Fig. 1. For linear region operation, the gate is biased to $V_G < 0$ to accumulate charges in the channel and the drain is biased to V_D = -0.1 V. In top-contact structure, the accumulation layer is induced not only in the channel but also at the bottom of overlap region. Under very small V_D, the sheet resistance R_{sh} of the accumulation layer can be considered to be uniform and the source and drain resistance can be considered to be equal, i.e., $R_{sd} = 2R_s$.

To derive I-V equation, the channel region is considered first as shown in Fig. 2. Due to the effects of R_{sd}, intrinsic source and drain voltages, V_S' and V_D', are different from the applied voltages. Using V_S' and V_D', the drain current I_{ds} can be expressed as

$$I_{ds} = \frac{W}{L}\frac{V_D'-V_S'}{R_{sh}} \approx \mu_{eff} C_i \frac{W}{L}(V_G - V_{TH})(V_D'-V_S') \quad (1)$$

where W, L, μ_{eff}, C_i and V_{TH} represent device width, device length, effective field-effect mobility, insulator capacitance and threshold voltage. For simplicity, R_{sh} itself is used in this paper for further discussion.

In Fig. 3, notations for the current and potential in the overlap region are shown. The electric potential and the current along the accumulation layer is represented by $V(x)$ and $I_x(x)$, respectively. From the source electrode to the accumulation layer, it is assumed that the current flows only in y-direction as represented by current density $J_y(x)$. R_y denotes the apparent y-direction resistance per unit area($\Omega\cdot cm^2$) which includes both contact and bulk semiconductor resistance. R_y is assumed not to depend on V_G because of the screening effect by the charges in the accumulation layer. Using Kirchhoff's law, three equations can be derived for the above physical quantities and solved as

$$J_y(x) = J_{y0}\exp(x/L_0) \quad (2)$$

$$I_x(x) = W L_0 J_{y0}\exp(x/L_0) \quad (3)$$

$$V(x) = -R_y J_{y0}\exp(x/L_0) \quad (4)$$

$$L_0 = \sqrt{R_y / R_{sh}} \quad (5)$$

where J_{y0} is an integration constant and L_0 is a characteristic length which is a function of V_G. It is hard to directly measure $J_y(x)$, $I_x(x)$ and $V(x)$, so simulation is used for verification. Fig. 4 compares the simulation results and the eq. (2), which shows good agreement for $J_y(x)$. For $I_x(x)$ and $V(x)$, similarly good agreements are obtained. From the above results, R_{sd} in the overlap region can be found as a function of L_0 as

$$R_{sd} = 2R_s = -2V(0)/I_x(0) = 2R_y/WL_0. \quad (6)$$

At the boundary of the channel and the overlap region, current should be continuous. Therefore, the relation

$$I_{ds} = I_x(0) \quad \Rightarrow \quad \frac{W}{L}\frac{V_D'-V_S'}{R_{sh}} = WL_0 J_{y0} \quad (7)$$

should be satisfied. Next, V_D consists of potential drops in the channel and two overlap regions. Therefore, the relation

$$V_D = 2V(0) + (V_D'-V_S') = -2R_y J_{y0} + (V_D'-V_S') \quad (8)$$

also should be satisfied. By solving eq. (7) and (8), the final I-V equation for top-contact OTFTs can be obtained as

$$I_{ds} = W\frac{V_D}{LR_{sh} + 2R_y/L_0}. \quad (9)$$

Eq. (9) converges to the general MOSFET equation if R_y = 0. If L = 0, R_{sd} in eq. (6) can be obtained again from eq. (9).

3. Device fabrication and discussion

To verify eq. (9), OTFTs are fabricated with different pentacene thickness as shown in Fig. 5. R_y is obtained using the admittance measurements and modeling of MIS capacitors [3] as shown in Fig. 6. Because R_y of 25 nm is relatively small, R_{sh} is obtained using the I-V curve of 25 nm device as shown in Fig. 7(a). Using the values of R_y and R_{sh} and eq. (5), L_0 of each device is obtained in Fig. 7(b). Finally, I_{ds} are calculated using eq. (9) and compared to the measured values in Fig. 8. The equation predicts the measured I-V curves with relatively small error. In Fig. 9, R_{sd} of the devices using eq. (6) and its ratio to the total resistance are depicted. The ratio is as large as 60 %, which shows significant influence of R_{sd} on OTFT performance.

4. Summary

An analytic I-V equation for top-contact OTFTs is derived including the effects of variable series resistance and

verified with fabricated OTFTs. These results can be useful for the further modeling of top-contact OTFTs.

Acknowledgements

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References

[1] D. J. Gundlach et al, J. Appl. Phys., **100** (2006) 024509.

[2] D. Natali et al, J. Appl. Phys., **101** (2007) 014501.

[3] E. J. Meijer et al, Appl. Phys. Lett., **78** (2001) 3902.

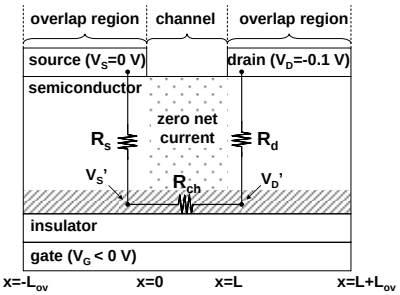


Fig. 1. The cross-section of a top-contact OTFT in the linear region. Accumulation layer is induced uniformly at the bottom of semiconductor due to the negative V_G. V_S' and V_D' represent intrinsic source and drain voltage, respectively. R_s, R_d and R_{ch} denote source, drain and channel resistance, respectively.

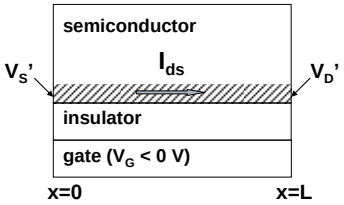


Fig. 2. For the channel, the current is determined by R_{sh} and the intrinsic source and drain voltage, i.e., V_S' and V_D'.

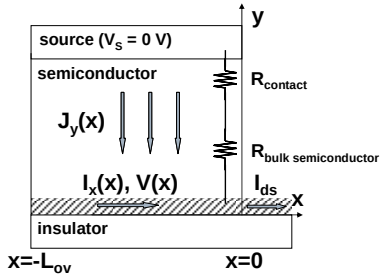


Fig. 3. For the overlap region, $I_x(x)$, $V(x)$ and $J_y(x)$ are determined by R_{sh}, R_y and Kirchhoff's law. For the current continuity, $I_x(x)$ becomes I_{ds} at x=0.

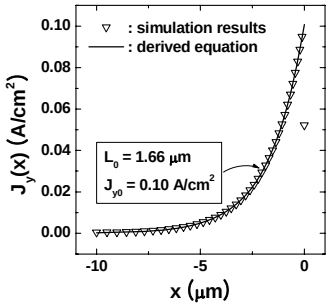


Fig. 4. To verify eq. (2), $J_y(x)$ is obtained from the simulation on an amorphous Si TFT. Good agreement between simulation and calculation shows that the equation for $J_y(x)$ is properly derived.

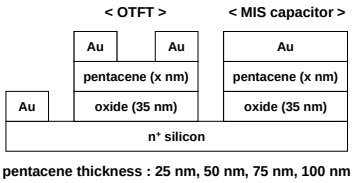
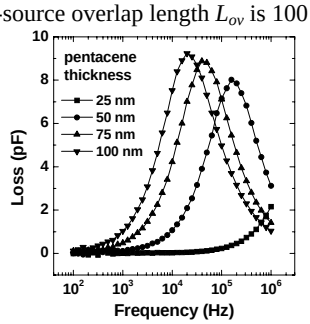


Fig. 5. The structure of the fabricated OTFTs and MIS capacitor. Pentacene thicknesses are varied to obtain different R_y. Gate-source overlap length L_{ov} is 100 μm.



pentacene thickness (nm)	R_y (MΩ·μm^2)
25	<46
50	426
75	1799
100	3923

Fig. 6. From the admittance measurements, R_y can be obtained with different pentacene thickness.

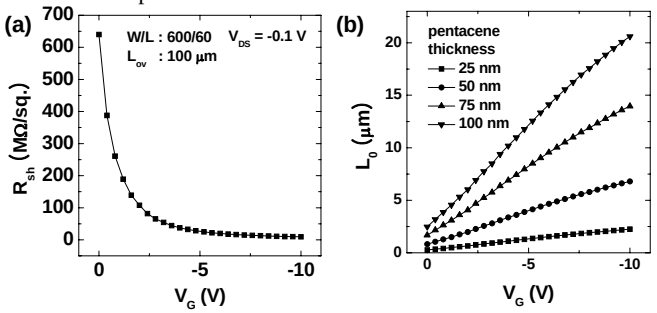


Fig. 7. (a) R_{sh} of the fabricated OTFTs. (b) L_0 of the fabricated devices which are calculated with eq. (5). L_0 is always smaller than the overlap length L_{ov} = 100 μm.

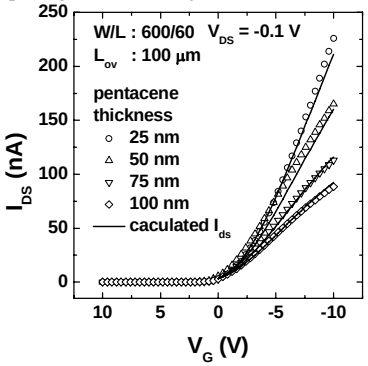


Fig. 8. The measured I-V curve (dotted line) and the calculated I-V curve (solid line) using eq. (9) show good agreement.

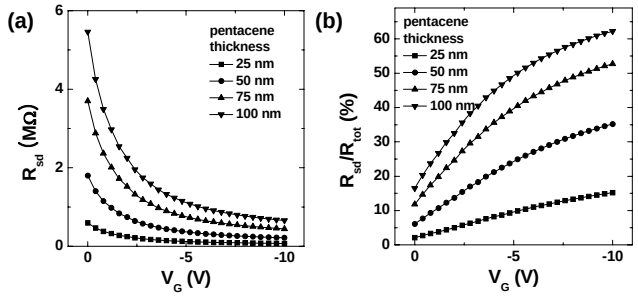


Fig. 9. (a) Obtained R_{sd} using eq. (6) (b) The ratio of R_{sd} to total resistance is as large as 60 % when pentacene thickness is 100 nm.