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Highly Reliable Bottom-Contact Pentacene TFTs with a Poly(*p*-chloroxylylene) Layer Selectively Grown on a Gate-Insulator

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1. Introduction

The shift in the threshold voltage (ΔV_{th}) under application of gate bias stress is one of the most important stability issues in organic TFTs (OTFTs) [1-4]. This bias stress instability (BSI) is mainly caused by the trapping of carriers in the channel into localized states in the semiconductor or at the semiconductor/gate insulator interface. For that reason, reduction of these trap states is essential to suppress the threshold voltage shift in OTFTs.

We report here a novel approach to improve the BSI by the selective growth of poly(*p*-chloroxylylene) (PPCX) on the surface of the gate insulator in bottom-contact (BC) pentacene TFTs. This method would passivate damage of the gate insulator surface caused by the manufacturing of source (S)/drain (D) electrodes, which improves the BSI of the OTFT remarkably.

2. Experimental

We made short-channel pentacene TFTs whose channel length (L) was 5 or 10 μm , which requires a BC structure to prevent damage to the semiconductor by solvents used in photolithography of S/D electrodes. Fig. 1 shows the process of manufacturing our pentacene TFTs. A 50 nm-thick gold gate electrode was made on a glass substrate by evaporation and conventional photolithography. Polyvinylphenol (PVP) with cross-linking agent was spin-coated on the substrate as a 310 nm-thick gate insulator. Then 50 nm-thick gold/platinum S/D electrodes were evaporated on the PVP gate insulator and patterned by conventional photolithography, as shown in Fig. 1(a). Subsequently, we deposited a 5 nm-thick PPCX layer by CVD at room temperature, as shown in Fig. 1(b). It is well known that there is incubation period

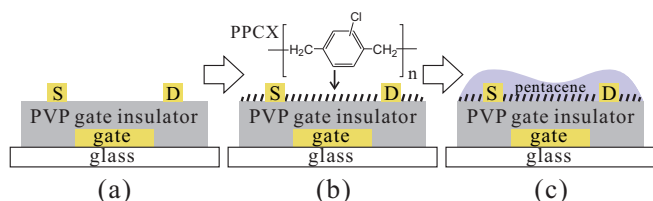


Fig. 1. Steps in processing of our device. (a) preparing glass substrate, patterning gate electrode and manufacturing source/drain electrode on PVP gate insulator made by spin coating (b) selective growth of PPCX on the PVP gate insulator (c) depositing pentacene.

for the growth of PPCX on certain metals but no incubation period for dielectrics [5]. PPCX can be selectively grown on a gate insulator but not on gold/platinum S/D electrodes within the period of incubation for gold and platinum. Note that the surface of the gate insulator in a BC structure is usually damaged by the photolithographic process to make S/D electrodes. PPCX can be selectively grown on this surface, which may have been damaged, and provides a clean gate insulator surface. Finally, a 50 nm-thick layer of pentacene was evaporated on the substrate, as shown in Fig. 1(c). We also prepared pentacene TFTs with a single-layer PVP gate insulator for reference. We investigated the BSI of these OTFTs in vacuum with pressure below 10^{-1} Pa.

3. Results and Discussion

Fig. 2 shows the time-dependent drain-current change of pentacene TFTs with a PPCX/PVP double-layer gate insulator and with a single-layer PVP gate insulator. The OTFT was constantly biased at gate bias stress of $V_{GS} = -30$ V and source-drain bias stress of $V_{DS} = -5$ V. The rate of drain-current change from the initial value to 1500 seconds stress time was 0.85-1.0% for the PPCX/PVP gate insulator and 5.6-9.3% for the PVP gate insulator.

Fig. 3 shows ΔV_{th} versus stress time based on the data in Fig. 2. The threshold voltage shift of the most reliable PPCX/PVP gate insulator OTFT was -0.14 V after 1500 seconds, which is one order of magnitude smaller than the corresponding value for the OTFT with the PVP gate insulator and even smaller than the value for

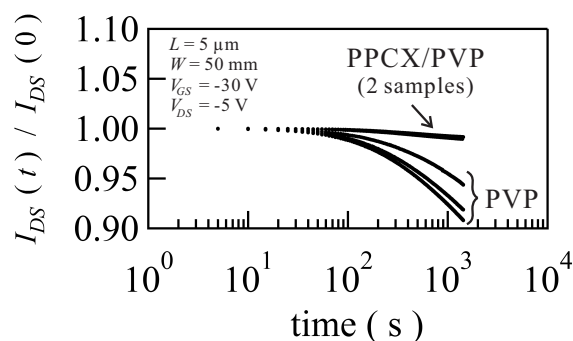


Fig. 2. The change of drain-current from the initial value to 1500 seconds stress time under a constant bias stress of $V_{GS} = -30$ V and $V_{DS} = -5$ V. $I_{DS}(t)$ is the drain current at stress time t and $I_{DS}(0)$ is the initial drain current. W is the channel width.

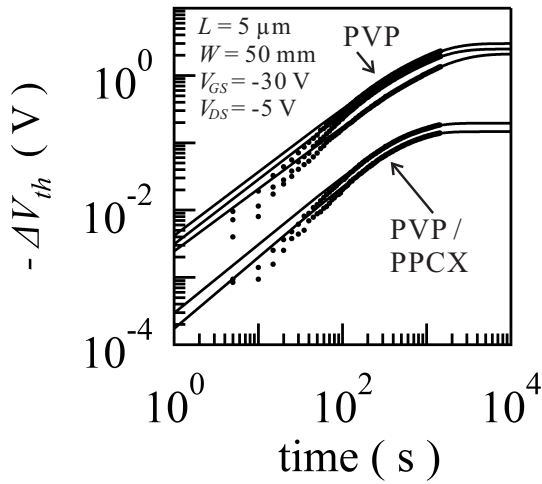


Fig. 3. The shift in the threshold voltage as a function of stress time under a constant bias stress of $V_{GS} = -30$ V and $V_{DS} = -5$ V. The solid lines were fit lines with the function (1).

an a-Si:H TFT [6].

In order to clarify the mechanism of the improvement of the BSI with PPCX gate insulator OTFTs, we estimated trap density in the channel. Fig. 4 shows transfer characteristics of 80 pairs of OTFTs with the PPCX/PVP gate insulator and with the PVP gate insulator. The average of subthreshold swing was 0.35 ± 0.07 V/decade for the PPCX/PVP gate insulator and 0.43 ± 0.16 V/decade for the PVP gate insulator. From the value of subthreshold swing, fast trap density can be estimated as $3.3 \pm 0.12 \times 10^{11} \text{ cm}^{-2}$ for the PPCX/PVP gate insulator and $4.3 \pm 1.2 \times 10^{11} \text{ cm}^{-2}$ for the PVP gate insulator [7]. The difference of these values cannot be responsible for the difference of ΔV_{th} between the PPCX/PVP gate insulator and PVP gate insulator.

The threshold voltage shift can be fit by the stretched-exponential function as [3,8],

$$\Delta V_{th}(t) = \Delta V_0 \left\{ 1 - \exp \left[- \left(\frac{t}{\tau} \right)^\beta \right] \right\}. \quad (1)$$

Here, t is a time. ΔV_0 is the threshold voltage shift at infinite time. τ is a characteristic trapping time of carriers. β is a weakly temperature-dependent dispersion parameter. A value of $C_g \Delta V_0 / e$ gives slow trap density, where C_g is the gate capacitance per unit area and e is the elementary electric charge. From the fit by the function (1), the slow trap density was estimated to be 1.0 - $1.4 \times 10^{11} \text{ cm}^{-2}$ for the PPCX/PVP gate insulator and 1.5 - $2.1 \times 10^{12} \text{ cm}^{-2}$ for the PVP gate insulator. This implies that the difference of threshold voltage shifts between the PPCX/PVP gate insulator and PVP gate insulator can be due to the difference of the slow trap density, which cannot be estimated from the subthreshold swings.

Fig. 5 shows AFM images of the 50 nm-thick pentacene film surface on the PPCX/PVP gate insulator and the PVP gate insulator. Because the average pentacene grain size on the PPCX/PVP gate insulator was smaller than that on the PVP gate insulator, pentacene film on the PPCX/PVP gate insulator has more grain boundaries than that on the PVP gate insulator. This result implies that the BSI of pentacene TFTs is dominated by trap

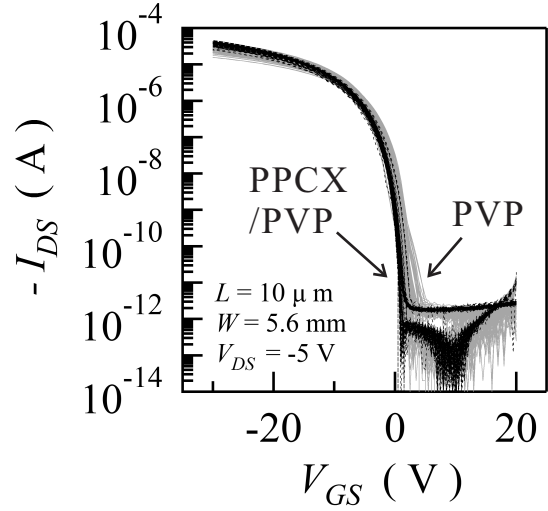


Fig. 4. Transfer characteristics of 80 pairs of OTFTs with the PPCX/PVP gate insulator and with the PVP gate insulator.

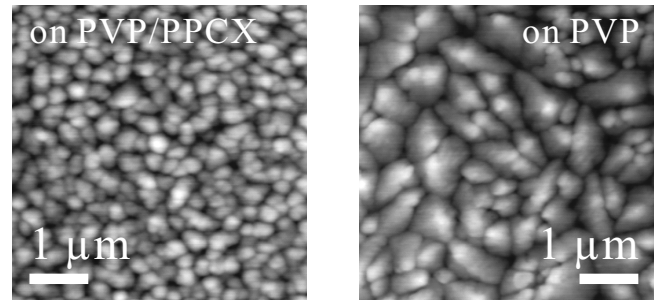


Fig. 5. AFM images of the 50 nm-thick pentacene film surface on the PPCX/PVP gate insulator and on the PVP gate insulator.

states at the semiconductor/gate insulator interface, but not by trap states at the grain boundaries.

With these results at hand, we consider that the improvement of the BSI of the pentacene TFTs with PPCX/PVP gate insulator can be attributed to the reduction of slow trap states between the semiconductor and gate insulator interface.

4. Conclusion

Highly reliable BC pentacene TFTs with low BSI have been achieved by introducing the PPCX layer selectively grown on the PVP gate insulator following the formation of S/D electrode. We found that the PPCX layer reduces the slow trap density of the semiconductor/gate insulator interface and consider that this is the origin of the improvement of the BSI.

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