Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 200-201

I-1-1 (Invited)

3D Stacked Nanowires CMOS Integration with a Damascene Finfet Process

T. Ernst[1], C. Dupré[1,2], E. Dornel[1], J.C. Barbé[1], S. Bécu[1], C. Vizioz[1], V. Delaye[1], F. Andrieu[1], J-M. Hartmann[1], S. Barnola[1], T. Poiroux[1], O. Faynot[1], G. Ghibaudo[2] and S. Deleonibus[1]

[1]CEA-LETI, 17 avenue des Martyrs 38054 Grenoble Cedex 9, France, email : thomas.ernst@cea.fr. Phone +33-4-38 78 23 33 – Fax +33-4-38 78 94 56

[2]IMEP, INPG-MINATEC, 3 Parvis Louis Néel, 38016 Grenoble Cedex 1, France,

Abstract

We present a morphological and electrical demonstration of CMOS devices with 3 and 4 stacked nanowires (30 to 70 nm). They showed an up to × 3.6 I_{ON} increase compared to a one-level trigate on SOI. The high current density/surface is obtained thanks to 3D integration. The integration process with an HfO_2/TiN gate stack is presented and discussed. The electron mobility is degraded by about 20% on nanowires with etched surfaces when compared to planar SOI devices. Results obtained by promising surface reconstruction processes for the rounding of suspended nanowires are presented as well.

Introduction

Short-channel effect control and the resulting OFF-state current increase is one of the main challenges that limits CMOS down-scaling. Various thin film architectures with an enhanced gate-channel coupling and a reduced source/drain-channel coupling [1] are thus explored in the literature to address the sub-32 nm technology nodes [2-6]. Indeed, compared to planar thin film transistors, the surrounding gate suppresses some parasitic source/drain-channel coupling [7] enabling very low leakage current.

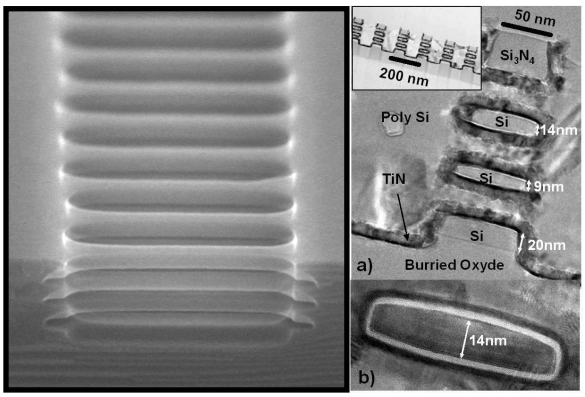

Fig. 1. Left: Three stacked levels nanobeam matrix after the Fin etch and the SiGe removal. Right: Cross sectional TEM pictures perpendicular to the beams of a) of one stacked Si channels, Inset: 3x50=150 beams b) of one Si channel: excellent Si crystalline quality is obtained; HfO_2, TiN and Poly-Si conformity is achieved.

Furthermore, the quantized width imposed by the nanowires structure may reduced significantly the driving current and/or the design flexibility compared to planar architectures. This limitation can be overcome by 3D approaches. 3D Gate-All-Around (GAA) demands some specific integration strategies [8-10]. In 3D Nano-Wire-GAA architectures (NWG), we use a combination of damascene-gate Finfet [11] and SON technologies [5,6] to obtain suspended nanowire with GAA HfO_2/TiN/PolySi gate.

Integration process

(Si/SiGe) superlattices were grown on top of SOI substrates [12]. After silicon nitride deposition, the superlattices are etched anisotropically in order to pattern fins 200-250nm thick and W_{min}=30 nm to 70nm wide.

Then the SiGe layers in-between the Si nanowires were selectively removed (Fig.1 left). Controlling the amount of etching species (fluorine radicals) leads to a slow and selective recess of the SiGe between the wires calibrated to liberate up to 70nm wide structures (SiGe partly remains for wider structures). HfO_2 and TiN films were then deposited [8]. Quasi-perfect step coverage is observed on NWG structures for both HfO_2 and TiN layers (fig. 1 right)

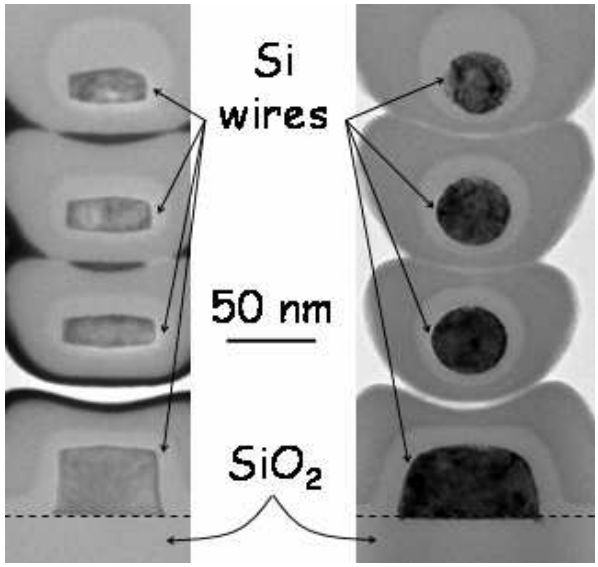

Figure 2: TEM cross section of the multilayers nanowires. (a) before annealing - not rounded nanowire (b) H_2 annealed at 850°C – rounded nanowires. The lower Si nanowires are on SiO2. Wires were capped with SiO_2, Si_3N_4 and W for TEM imaging purposes.

After the deposition of 350 nm n+-doped poly-Si the structures were planarized thanks to chemical mechanical polishing down to the aforementioned Si_3N_4 layer (on top of the superlattices). Then, the gate contact was etched. The gate is self-aligned and its length is defined by the distance between the source and drain blocks.

Rounded suspended nanowire

By introducing optimized hydrogen annealing, we obtained rounded and continuous suspended nanowires. Hydrogen annealing was used intentionally for 3-D profile transformation by rounding sharp corners while diminishing surface roughness [13]. The improved surface roughness has further been shown to enhance the electrical characteristics of FinFETs [14].

Current gain and mobility analysis (not-rounded nanowire)

Well-behaved sub-threshold and linear current characteristics were measured on NMOS and PMOS transistors with 0.7µm gate length (Fig. 3 and 4). The reproducibility of the characteristics was confirmed by statistical measurements [7].

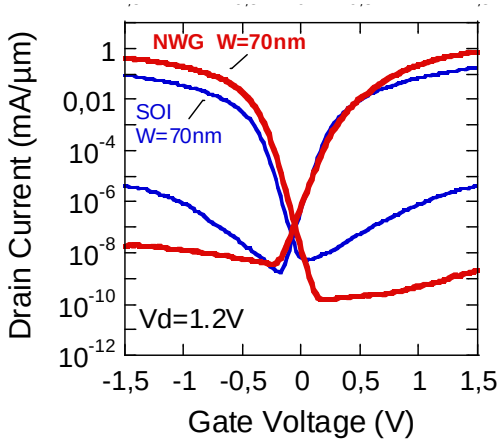

Fig. 3. Id(Vg) characteristics of 3D nanowires (Lg=0.7µm) compared to planar trigate for the same width W. V_T are normalized for SOI.

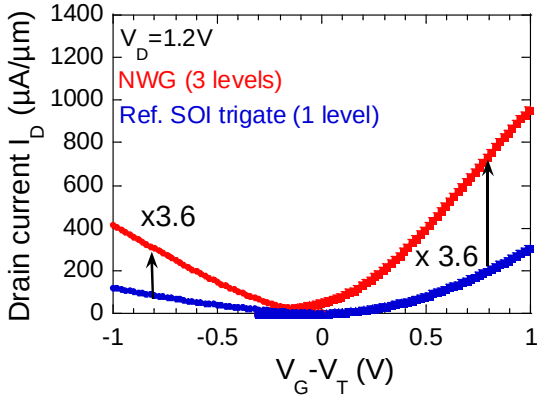

Fig. 4 Current comparison between NWG and planar SOI normalised by W. Current gains are given for $|V_G-V_T|$= 0.8V, L=0.7µm.

Let us consider the current gain per surface of layout. A current gain density up to a factor 3 is obtained compared to a one level trigate structure.

$$W_{eff,trigate} = W_P + 2t_{Si}$$

$$W_{eff,NWG} = 2(n-1)(W_P + t_{Si}) + W_P + 2t_{Si}$$

where n is the stacked nanowire number and t_{Si} is the Si film thickness, $W_{eff,trigate}$ is the effective width for trigate device and $W_{eff,NWG}$ for NWG. The ideal gain on such architecture should be the ratio between $W_{eff,NWG}$ and $W_{eff,trigate}$ i.e 5 in our 3 nanowire level structure. Analytical modelling of the gain reveals dependences on mobility, equivalent capacitance gate oxide thickness, access resistance, gate and drain voltage [15, 16] which explain the non-constant gains measured experimentally.

The electron mobility is degraded for NWG compared to trigate SOI (see Fig. 5). This is probably due to an enhanced surface roughness and interface charges scattering due to surface Si etching.

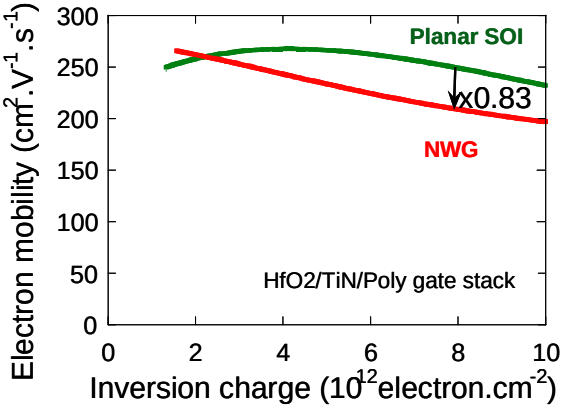

Fig. 5. Measured p-channel mobility for NWG and trigate SOI versus measured inversion charge

Conclusion

We successfully fabricated and characterized 3D stacked nanowires CMOS transistors. Our damascene gate process demonstrated a self-aligned integration and well-controlled nanowire dimensions. The measured current gain compared to planar SOI can reach a factor 3.6. Detailed mobility analysis of such devices will provide further understanding of GAA transport properties.

References

[1] C.W-Lee et al.., Solid-State Electronics vol. 51, pp. 505–510, 2007
[2] D. Hisamoto et al. , IEEE TED, vol. 38, p 419, 1991
[3] M. Vinet, IEEE Trans. Nanotec., vol.5, n°6, pp 643, 2006
[4] F. Andrieu et al, VLSI Tech Symp, 4A-5, 2007
[5] S. Monfray et al., VLSI Tech., p. 108-109, 2002
[6] S. Harrison et al, IEDM Tech. Dig., p. 18.6.1-18.6.4, 2003.
[7] T. Ernst et al. Vol. 54, n° 6, p. 1366, 2007
[8] S.-Y. Lee. et al. , VLSI Tech Symp, p.200, 2004
[9] M.-S. Kim et al., VLSI T. Symp, p.84, 2006
[10] T. Ernst et al, IEDM 2006
[11] D. Hisamoto, IEEE TED, vol. 47, n° 12, dec 2000
[12] J.M. Hartmann et al, J. Cryst. Growth 283, 57, 2005
[13]] M.-C. M. Lee and M. C. Wu, J. MEMS 15(2), 338 (2006)
[14] W. Xiong et al., IEEE Electr. Dev. Lett. 25(8), 541 (2004)
[15] C. Dupré et al ULIS 2007 proceedings.
[16] E. Bernard et al., to be published

Acknowledgements

This work was carried out under the French Ministry of Research Institut Carnot program