

I-1-2

3D Multi-gate NMOS Mobility Enhancement with High-tensile ILD-SiN_x Stressor

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1. Introduction

To achieve ultra-high density, 3D multi-gate transistors have emerged as a promising candidate as compared with other double gate device structures due to their process compatibility with traditional logic devices [1~3]. Moreover, 3D multi-gate devices present the following advantages: (1) Shallow trench isolation is not needed, (2) Device DIBL or short channel effect can be effectively improved due to increased gate control on the channel region on the ultra thin silicon body of Si-fin. It is also known that in order to improve the drive current of a conventional planar NMOS, a highly tensile ILD nitride layer can be used to enhance the N-channel carrier mobility. [4~6] Hence, in this work we developed a high aspect ratio 3D multi-gate device with a high-tensile strained channel area through a thick high-tensile ILD-SiN_x stressing film and NMOS multi-gate device achieves significantly enhanced mobility and drive current performances.

2. Device Fabrication

SOI wafers were used with a traditional ULSI sub-65nm generation logic technology to fabricate high-aspect-ratio 3D multi-gate NMOS devices. The SOI wafer with a (110)-orientated crystalline silicon (c-Si) layer was thinned down using oxidation-and-etching steps and the final c-Si thickness was controlled to 85~95nm. The last oxidation process was selected to obtain an appropriate oxide layer for the subsequent Si-fin definition to achieve a desirable Si-fin width. A sacrificial thin oxide was then grown on both sides of the vertical sidewall to serve as a screen oxide and to remove etch damage near the Si-fin surface. Subsequently, boron (B) and arsenic (As) ions based on simulation results with a tilted angle were used for threshold voltage (V_{th}) adjustment of NMOS and PMOS multi-gate devices.

After threshold implantation, the screening oxide was removed followed by the growth of a 14Å (physical thickness) plasma nitrided oxide as the gate dielectric. Subsequently, an un-doped polysilicon (poly-Si) gate layer was deposited. Then, a high dosage phosphorus (P) implantation was rendered for the NMOS poly-Si gate area. To achieve a poly-Si gate length target of 80nm, an oxide hard mask and a 193nm scanner were used. After the gate spacer formation, both the N⁺ (As) and P⁺ (B) source/drain ion implantation were conducted. Next, a cobalt salicide process was used followed by removal of gate SiN_x spacer and subsequent deposition of a thick highly tensile strained

(1.41GPa) CVD ILD-SiN_x capping layer. A standard ILD-SiO₂ deposition and tungsten contact filling processes were then followed by a copper interconnect process. Finally, a passivation layer was deposited followed by formation of aluminum bonding pads.

3. Results and Discussions

Fig. 1 displays the wafer x-axis X-TEM pictures of a 3D multi-gate CMOS device after integration with a 110nm-thick highly tensile ILD-SiN_x capping layer.

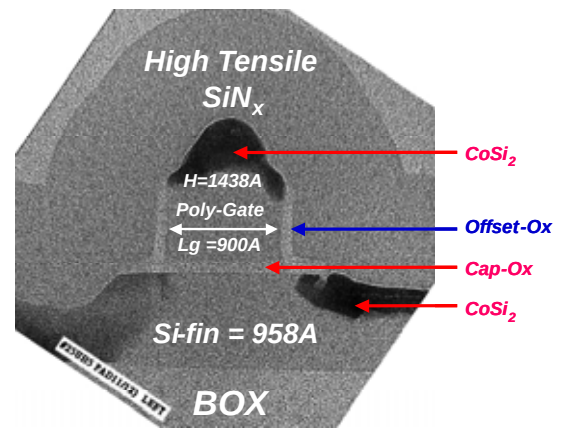


Fig. 1 The x-axis X-TEM pictures of a 3D multi-gate CMOS device integrated with a high tensile ILD-SiN_x capping layer.

The universal I_{off} versus I_{on} plot in **Fig. 2** shows a significantly improved drive current of $\sim 100\mu A/\mu m$ (+26% current gain) at the same I_{off} current of $1E-8$ Amp/ μm can be achieved for the highly tensile strained (1.41GPa) NMOS multi-gate devices.

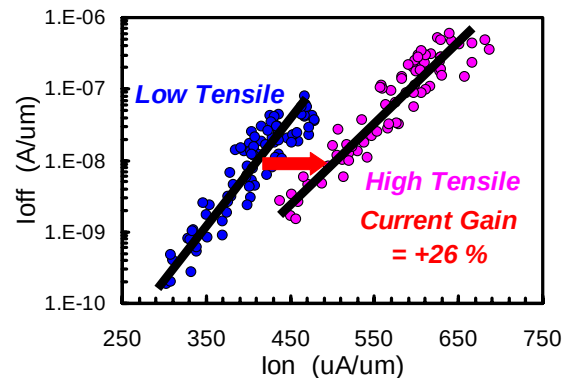


Fig. 2 I_{off} versus I_{on} curves of the high tensile and conventional low tensile 3D multi-gate NMOS devices.

Fig. 3 display that for the conventional low-tensile strained 3D NMOS with Si-fin width (W) / gate length (L) / Si-fin height (H) = 22/90/96nm at $V_d=V_g=1.0V$, its $I_{d,sat}=527\mu A/\mu m$, subthreshold swing (Swing) = 65mV/decade, and DIBL=0 mV/V; whereas for the highly tensile stressed 3D NMOS with the same device dimensions, a relatively high I_{on} of $771\mu A/\mu m$ can be achieved and the original excellent Swing and DIBL performance of the low tensile strained 3D NMOS are still maintained.

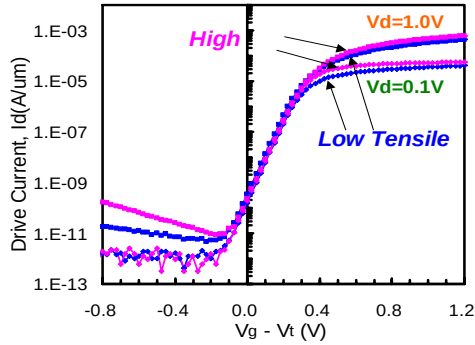


Fig. 3 I_d - V_g transfer curves of $L_g=90nm$ high tensile and conventional low tensile NMOS multi-gate devices.

Fig. 4 displays that for the gate length $L_g=90nm$ high tensile 3D NMOS multi-gate device a distinct current gain of 34% (increasing from 540 to $722\mu A/\mu m$) can be achieved at $V_d=V_g=1.0V$.

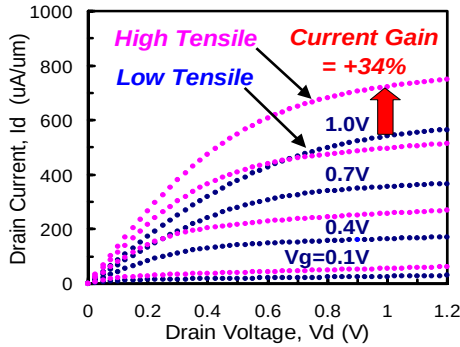


Fig. 4 I_d - V_d characteristic curves of $L_g=90nm$ high tensile and low tensile NMOS multi-gate devices.

Moreover, **Fig. 5** depicts relatively high n-channel mobility for the high-tensile multi-gate device with gate length of 90nm, which is also consistent with the previously mentioned simulation and drive current enhancements.

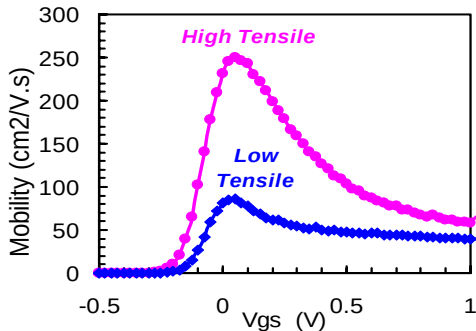


Fig. 5 The extracted n-channel mobility of $L_g=90nm$ high tensile and low tensile NMOS multi-gate devices.

Fig. 6 depicts the maximum transconductance ($G_{m,max}$) measured at $V_d=0.1V$ for 3D NMOS devices with varied gate lengths and indicates an enhancement of $G_{m,max}$ for the highly tensile strained NMOS multi-gate channels below the gate length $L_g=2\mu m$, which also reveals the relation to the significantly increased n-channel mobility and drive currents.

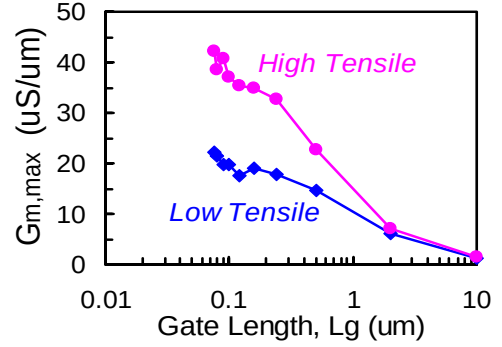


Fig. 6 The $G_{m,max}$ of high tensile and conventional low tensile 3D NMOS multi-gate devices.

Additionally, **Fig. 7** demonstrates that the DIBL of highly tensile 3D NMOS multi-gate devices is also improved as compared to that of the conventional low stress 3D multi-gate NMOS devices, which also indicates an even better short channel suppression performance.

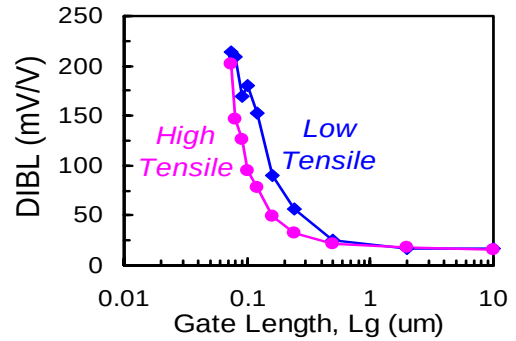


Fig. 7 The DIBL of high tensile and conventional low tensile 3D NMOS multi-gate devices

4. Conclusions

3D multi-gate NMOS devices with ultra-high aspect ratio (>7) have been successfully integrated with a thick highly tensile CVD nitride stressor film as the first ILD sealing layer and demonstrates promising device performance enhancements. Moreover, gate length of 90nm exhibit drastically improved channel mobility, transconductance (G_m), and DIBL performances. The I_{off} - I_{on} universal curves also displays an extraordinary drive current (I_{on}) gain of 26% with the device off current $I_{off}=1E-8$ Amp/um.

References

- [1] J. Kedzierski, et al., IEEE-ED, v.50, n.4, p.952~958, 2003. .
- [2] B. Yu, et al., IEDM 2002, p.273~276.
- [3] F. L. Yang, et al, Symp. VLSI Tech., 2002, p.104~105.
- [4] S. M. Cea, et al., IEDM 2004, p.963~966.
- [5] K. Goto, et al., IEDM 2004, p.209~212.
- [6] S. Pidin, et al., IEDM 2004, p.213~216.