Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 204-205

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The Drivability Enhancement Mechanisms in Nano-grating MOSFETs

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1. Introduction

Higher drivability of transistors is indispensable to meet the requirement of electronic system, while as the device dimensions shrink to the nanometer region, several effects observed in short channel devices have threatened to prevent the scaling of conventional MOSFET. So an ultra-shallow multi-wall channel structure called nano-grating MOSFET was proposed to enhance the current drivability without scaling the channel lengths down [1, 2]. The nano-grating MOSFETs are fabricated by conventional process with the silicon wafer having periodic nano-gratings shallower enough than the site flatness requirement, as seen in ITRS2005, by which good area advantage and wider effective channel width than that of a conventional MOSFET with the same mask-defined width and length can be achieved. In this work, the drivability enhancement mechanisms of nano-grating devices are analyzed and the different effects in nMOSFET and pMOSFET are shown.

2. Experiments

Both the nano-grating and conventional MOSFETs including n-type and p-type are employed for this experiment. For both the nano-grating nMOSFET and pMOSFET, the trench structure with grating pitch of 140 nm and height of 35 nm were formed by reactive ion etching (RIE) on Si substrates with (100) surface. After that, the nano-grating MOSFETs and conventional ones are fabricated with the same process without caring about the nano-grating structure. The SiON gate insulator layer of 2 nm was formed with a nitric oxide (NO) gas atmosphere at 800℃ after dry oxidation. The poly Si gate electrode was deposited and followed by patterning, dopant ion implantation and annealing. The standard contact metallization steps completed the device fabrication. Figure 1 shows the structure of a nano-grating MOSFET. The current flows along three kinds of surfaces of silicon, i.e., on the top, bottom and sidewall of each grating, which results in an effectively-enhanced channel width. The enhancement of drain current by using the nano-grating channel structure was confirmed in electrical characteristics. And the temperature dependence of mobility characteristics was also investigated.

3. Results and Discussions

Figure 2 shows the I_d-V_{ds} characteristics of nMOSFET and pMOSFET with conventional and nano-grating channels, at measurement temperatures of 233K and 473K with gate voltage V_{gs}=1V or -1V. An increase of I_d current in both n-type and p-type nano-grating device at any measurement temperature was confirmed, so the nano-grating channel structure can be considered to be effective. The I_d increase, however, may be caused by changes in threshold voltage, mobility, gate-oxide thickness as well as channel width. The threshold voltage of nano-grating device was smaller than that of conventional one, while the gate insulator was little thicker than conventional device resulting in a smaller enhancement of effective channel width. To analyze the mechanisms of the enhancement of drain current I_d, the effective channel mobility in the inversion layer of both nano-grating and conventional MOSFETs at different measurement temperatures was investigated and results are shown in Fig.3 and 4. Figures 5 and 6 show the peak effective mobility at different measurement temperatures in the nano-grating and conventional MOSFET of n-type and p-type. The peak mobility degradation caused by temperature dependence of phonon scattering has been observed in both nano-grating and conventional devices, although the degree is different. The temperature dependency is found to be approximated by $T^{-3/2}$.

The current flow direction in both nano-grating and conventional device is <110>, but in nano-grating device the channel region is formed on horizontal (100) and vertical (110) surfaces. The <110> on (110) gives smaller electron mobility and larger hole mobility than those of <110> on (100) [3], which was considered to be the reason to explain the mobility difference in nano-grating and conventional MOSFET at lower measurement temperatures. With the rise in measurement temperature, the difference between nano-grating and conventional MOSFETs became smaller, which is considered to be due to the fact that the surface orientation dependence of the carriers' effective mass becomes smaller at high temperature [4]. And the stress due to the poly-Si gate that filled the spaces between the walls in nano-grating device may result in the difference in mobility between nano-grating and conventional MOSFET at the high temperature of 473K.

Table 1 shows the transconductance enhancement at different measurement temperatures by using nano-grating channel structure with the overdrive voltage of 1V. It is obvious that with the rise of measurement temperature, the enhancement is becoming closer to the enhancement expected by the increase in the effective channel width, which is about 35%.

4. Conclusion

The drivability of both n-type and p-type nano-grating channel MOSFETs can be enhanced without any additional process except the formation of nano-grating. Because of (110) sidewall, the stress induced by the poly silicon gate, and the phonon scattering of carriers, enhancement of the drivability in nMOSFET becomes larger, while in pMOSFET smaller with the increasing temperatures.

References

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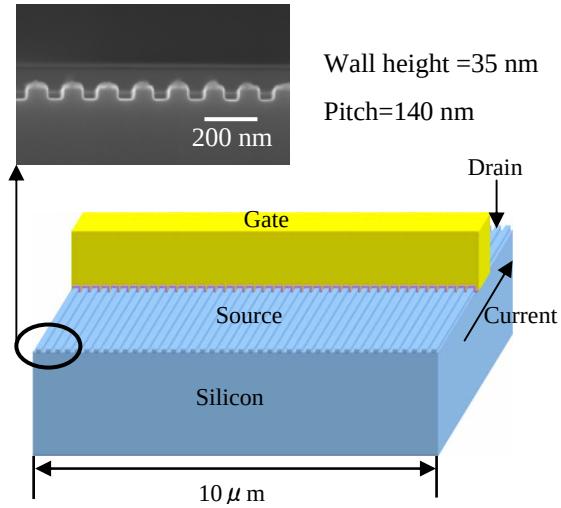


Fig.1 Structure of a nano-grating MOSFET.

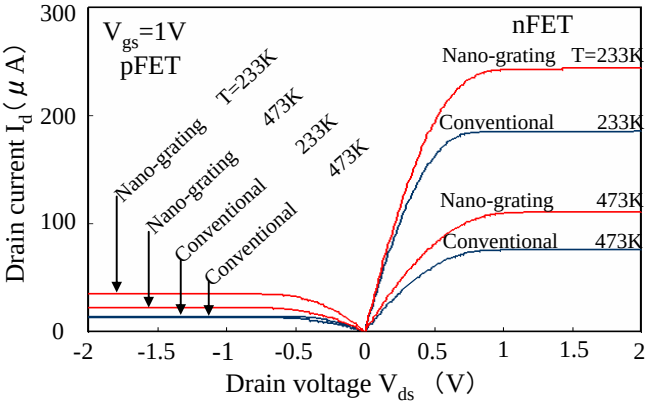


Fig. 2 The Id-Vds characteristics of nano-grating and conventional MOSFET with the same channel length of 10 μm and the same plain channel width of 10 μm at measurement temperature of 233K and 473K.

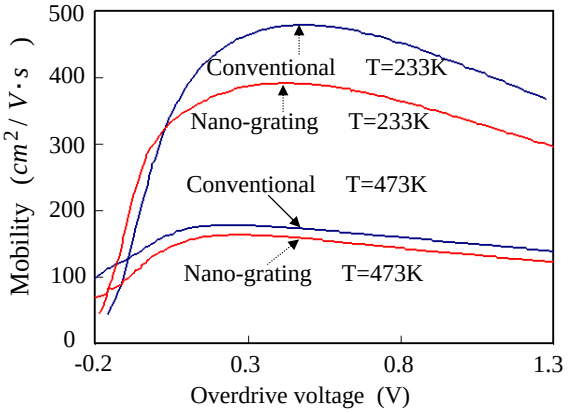


Fig. 3 The mobility in nano-grating and convetional nMOSFET at different measurement temperatures.

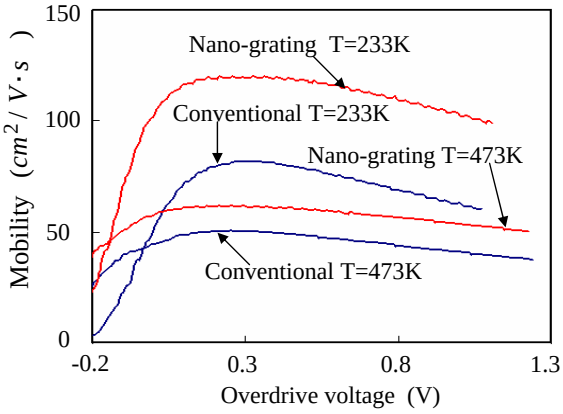
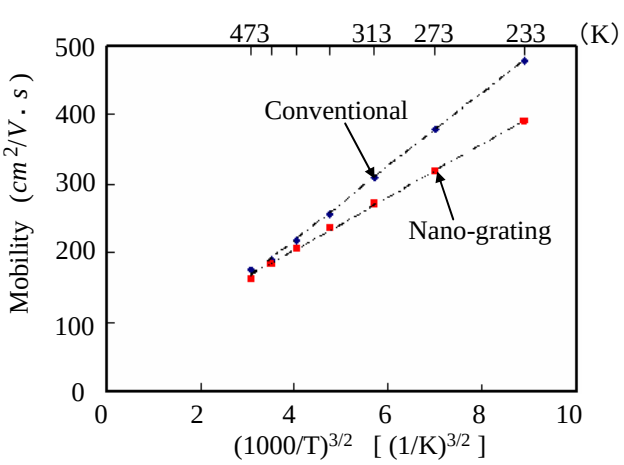


Fig. 4 The mobility in nano-grating and convetional pMOSFET at different measurement temperatures.



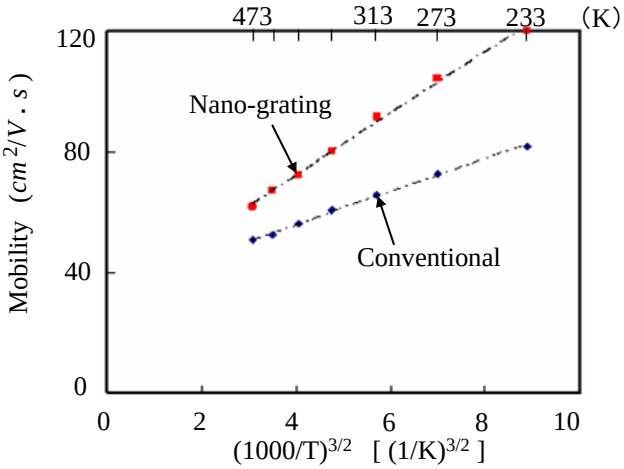


Fig.5 The temperature dependence of peak mobility in nMOSFET. Fig.6 The temperature dependence of peak mobility in pMOSFET.

Table 1 Temperature dependence of transconductance enhancement by using nano-grating channel structure at the overdrive voltage of 1V

Temperature (K)	Enhancement of transconductance (%)			
	NMOS		PMOS	
	W=10 μm, L=10 μm	W=5 μm, L=0.25 μm	W=10 μm, L=10 μm	W=5 μm L=0.25 μm
233	2.57	17.27	136.80	55.20
313	10.77	20.70	112.40	53.99
473	19.23	22.64	82.44	43.30