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Low Contact Resistance with Low Schottky Barrier for N-type Silicon Using Yttrium Silicide

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I. Introduction

As the current drivability of MOSFETs increases, source/drain series resistance (R_{SD}) seriously limits their performance [1]. In order to reduce R_{SD}, it is important to reduce contact resistance [2]. To achieve lower contact resistance, Schottky Barrier Height (SBH) between silicide and silicon must be low, for example ~0.3eV or less. A dual metal silicide structure, using low work function silicides for n^+ silicon and high work function silicides for p^+ silicon, is a promising solution [2]. In another approach, Schottky Barrier MOSFET (SB-MOSFET) also attracts much attention due to its inherently low R_{SD} [3]. This device also requires a low SBH for n or p type silicon. Therefore, the technology for controlling SBH is strongly required both for p and n type silicon. At present, however, there is no suitable candidate that has a low SBH for electrons.

Rare Earth silicides (RE silicides) are the most promising material to have a low SBH for electrons [4, 5]. In this paper, we study a high quality Yttrium silicide formation process using N_2 ambient cleaning and transfer technology.

II. Experimental

In order to evaluate the SBH between Yttrium Silicide and n-type and p-type silicon, Schottky Barrier diodes were fabricated. N on n^+ and p on p^+ EPI Si(100) wafers were prepared, having the resistivity of around 10Ωcm in the epitaxial layer and 10^{-2}Ωcm in the substrate, respectively. A-300nm-thick field oxide layer was formed at 1,100°C by wet oxidation. Typically 100μm×100μm square windows were opened in the field oxide. Then the wafers were cleaned by total room temperature 5 step cleaning [6]. Chemical oxide was formed by dipping in O_3 dissolved ultra pure water. After that, the wafers were loaded into a N_2 sealed cleaning chamber. After removing the chemical oxide with a diluted HF solution, the wafers were transferred to clustered sputter equipment in an N_2 ambient as shown in Fig. 1. 20nm of Yttrium film was formed by rf sputtering deposition, followed by ramp annealing to form Yttrium silicide. Sputtering conditions are listed in Table 1. A 400-nm-thick Al electrode was deposited on it also by rf sputtering. Finally, back contact was formed by Al evaporation. SBH was evaluated mainly from current- voltage characteristics.

III. Results and Discussions

Measured resistivity of Yttrium film is listed in Table 2. Measurement was performed in N_2 ambient. Relatively high resistivity was obtained, and the values don't change significantly even if the film is not exposed to air. Probably this high value isn't due to oxidation of Yttrium film by exposed to air, but its columnar grains as observed from above cross-sectional SEM image. Fig.2 shows the sheet resistance and resistivity of Yttrium silicide film as a function of the annealing temperature. In this experiment, we prepared SOI substrate in order to avoid the effect of substrate resistance. The sheet resistance rapidly fell at a temperature of over 350°C, which implies silicidation reaction began at around this temperature. Fig.3 shows XRD patterns of Yttrium silicide film as a function of the annealing temperature. The diffraction peaks of Yttrium were not detected at over 350°C, while Yttrium disilicide peaks were found at over this temperature, which agrees well with the result of the sheet resistance shown in Fig. 2. Although YSi_2 peaks were detected, it should be noted that RE silicides tend to form silicon-insufficient-disilicide phase such as YSi_{2-x} [7]. Fig. 4 shows the JV characteristics of Yttrium gate Schottky barrier diode both for p and n type silicon. Extracted SBH for electrons was 0.40eV while SBH for holes 0.68eV. The sum of them was about 1.08eV, almost equal to the bandgap of silicon (1.1eV). Also, an n-value of 1.02 was obtained, which implies good interface property between Yttrium and silicon. Fig. 5 shows the JV characteristics for Yttrium silicide gate Schottky barrier diode for p type silicon. Annealing time was 2minutes for all samples. For lower annealing temperature such as 400°C or 500°C, the SBH for holes became lower. By annealing at 600°C, we obtain the SBH value of 0.67eV, implying the SBH for electrons is about 0.4eV. By using such low SBH for electrons, the lower contact resistivity will be achieved.

IV. Conclusion

We have fabricated Yttrium and Yttrium silicide gate Schottky barrier diode on Si(100). In order to realize an ideal metal/silicon interface, silicon wafers were cleaned and transferred in an N_2 ambient without being exposed to air. Al/Y/p-type silicon Schottky barrier diode showed an excellent n-value of 1.02. The measured SBH for p-type silicon is 0.68eV (Yttrium) and 0.67eV (Yttrium silicide), respectively. This paper gives the key technology for fabricating low Schottky barrier for n-type silicon using Yttrium and its silicide, and can be applied to the formation of other promising RE silicides such as $ErSi_x$, $YbSi_x$.

Acknowledgments

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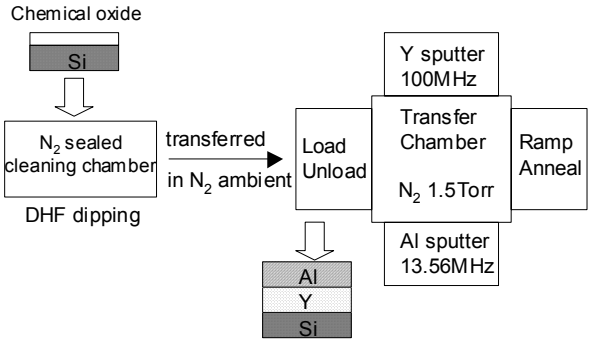
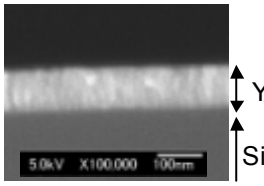


Fig.1 Concept of an N_2 ambient cleaning and transfer system.
In N_2 sealed cleaning chamber, measured oxygen concentration was about 20ppm, corresponding dissolved oxygen concentration in UPW was about 0.9 ppb calculated from Henry's law. Base pressure of both sputter chambers were ~10^{-7}Pa (10^{-9}Torr)

	in-situ surface cleaning	deposition
Gas	Ar	Ar
Flow Rate	432 sccm	216 sccm
Pressure	1.3Pa (10mTorr)	0.67Pa (5mTorr)
Substrate Temperature	RT	RT
RF Power	10W	100W
Time	1min	1.3min (20nm)

Table 1. Sputtering conditions of Yttrium films



Measured in N_2 ambient
(O_2 conc. ~20ppm)

Condition	Resistivity [μΩcm]
without exposed to air	177
left in air for 10min	179
left in air for 2h	182

Table 2 Measured Resistivity of sputtered Yttrium film. Considering its easily-oxidized property, wafer handling and measurement were performed in an N_2 ambient. The measured value slightly changed by being exposed to air, but seems not to be a main reason for such high resistivity.

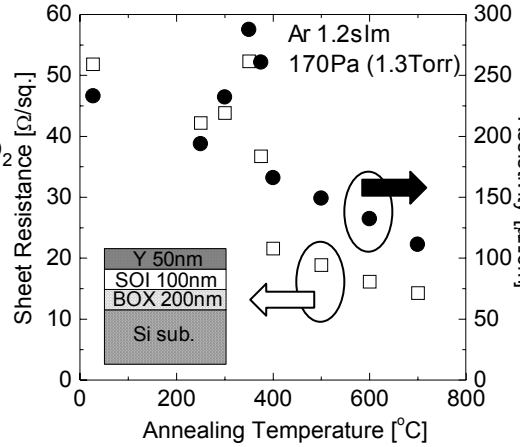


Fig.2 Sheet resistance and resistivity of Yttrium Silicide film as a function of the annealing temperature. Deposited thickness of Yttrium film was 50nm. Assuming that formed Yttrium silicide is uniform, the resistivity ρ was calculated as $\rho = R_S \times d$, where R_S is measured sheet resistance and d thickness measured by SEM observation, respectively.

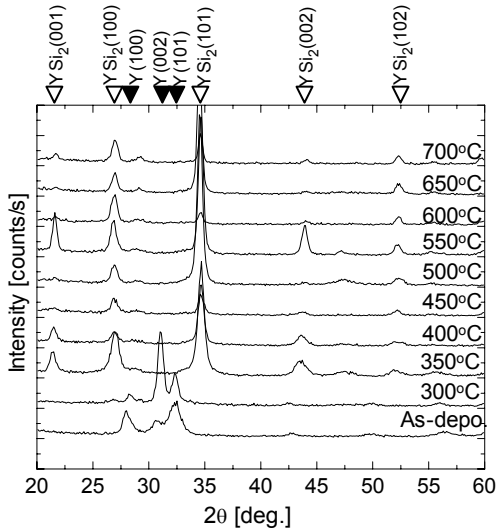
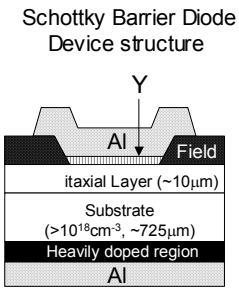


Fig.3 XRD patterns of Yttrium silicide film as a function of the annealing temperature. 200nm Y film was deposited on Si substrate followed by ramp annealing at several temperature for 2minutes. The diffraction peaks of Yttrium were not detected at over 350°C, while Yttrium disilicide peaks were found over this temperature.



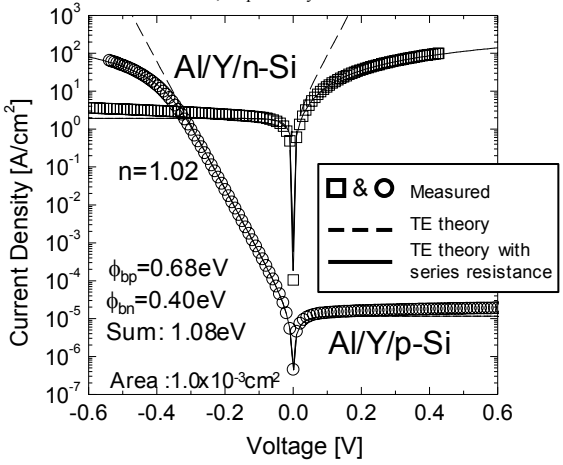


Fig.4 JV characteristics of Yttrium gate Schottky barrier diode both for p and n type silicon. The schematic view of fabricated Schottky barrier diode is also shown in the left. Note that the surface dopant concentration was controlled to be ~2×10^{16}cm^{-3} by P+/B+ implantation. The Al electrode also acted as an oxidation prevention layer for Yttrium and its silicide, which are easily oxidized in air. Measurement was performed at 300K. Extracted series resistance was 2.5Ω for p-type substrate and 3.5Ω for n-type substrate, respectively.

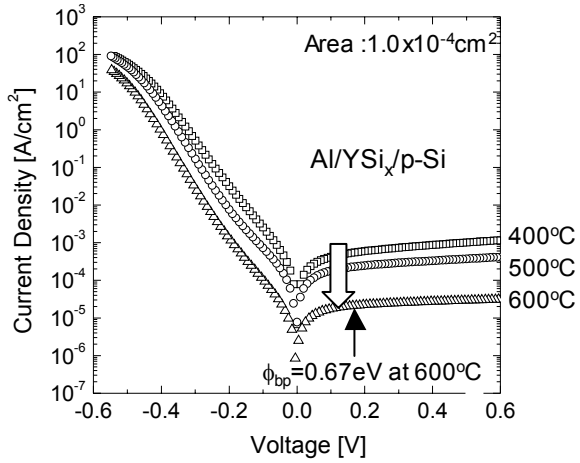


Fig.5 JV characteristics of Yttrium silicide gate Schottky barrier diode for p type silicon. Annealing time was 2 minutes for all samples. For lower annealing temperature such as 400°C or 500°C, the SBH became lower. By annealing at 600°C, we obtain the SBH value of 0.67eV.