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Double-Spacer Impact-ionization MOS Transistor: Characterization and Analysis

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ABSTRACT

In this paper, the Impact-ionization MOS (I-MOS) transistor structure is further optimized by utilizing a double-spacer for the formation of shallow source and lightly-doped drain. The shallow source extension lowers the breakdown voltage needed for avalanche breakdown, and the lightly-doped drain extension reduces the impact of drain bias on breakdown voltage and hence the threshold voltage. The double-spacer I-MOS is fabricated and characterized. Detail analysis and physical explanation to the impact of drain/gate bias on the device characteristics are laid out. In addition, excellent subthreshold swing and good device performance are achieved.

1. INTRODUCTION

The Impact-ionization MOS (I-MOS) transistor has been proposed as an alternative device to alleviate the power consumption issue faced by CMOS device scaling. The main advantage of such a gated p-i-n diode transistor is that it is able to achieve sub-60 mV/decade subthreshold swing at room temperature. Various groups have demonstrated the feasibility of realization such a p-i-n diode structure using different fabrication methods [1]-[3].

In this paper, we realize a lateral I-MOS structure using a double-spacer technique to form the impact-ionization region (I-region) and source/drain region. The proposed structure allows further fine-tuning and improvement of the device performance.

2. DEVICE STRUCTURE AND CONCEPT

The basic lateral I-MOS structure is shown in Fig. 1(b). Unlike the conventional MOSFET [Fig. 1(a)], the I-MOS transistor has an asymmetrical structure. For an n-channel device, the drain is doped n^+, while the source is doped p^+. During device operation, the source is at a negative bias whereas the drain is at a positive bias. The gate voltage controls the avalanche breakdown of the p-i-n diode and results in huge on-current to flow from the source to drain when the critical electric field is reached. Fig. 2(a) shows the simulated gate transfer characteristics of a MOSFET and an I-MOS device. Conventional MOSFET conducts current through the thermal injection of carriers from the source, and is limited by the Fermi-Dirac distribution of carrier energy [Fig. 2(b)]. Thus, the subthreshold swing is limited to 60 mV/decade at room temperature. However, current conduction in I-MOS has an abrupt dependence on the electric field in the I-region [Fig. 2(c)], giving sub-60 mV/decade swing, excellent I_{on}/I_{off} ratio, and high performance with low power consumption.

In order to optimize the I-MOS performance, a double-spacer (DS) I-MOS is realized (Fig. 3). A lightly-doped drain extension implant is employed to reduce the effect of drain bias on the breakdown voltage V_{BD} and threshold voltage V_T. Similar to the drain-induced barrier lowering (DIBL) in MOSFET, the lightly-doped drain extension reduces the drain-induced breakdown voltage lowering (DIBVL) in DS I-MOS. TCAD simulation shows that it improves the control of short channel effects (DIBVL = 0.1 V/V), as compared to the basic I-MOS structure (DIBVL = 0.4 V/V). The 1st spacer is used to define the length of the I-region, L_I. A shallow source extension implant is employed to from a more abrupt junction to reduce V_{BD} of DS I-MOS [4]. In order to reduce the high series resistance due to the shallow source extension, a 2nd spacer is defined for the formation of the deep source implant. Similarly, the drain is also heavily doped to reduce the drain series resistance. A summary of the process modifications is shown in Table 1.

3. DEVICE FABRICATION

The process sequence for the realization of the DS I-MOS is depicted in Fig. 4. 8-inch Silicon-On-Insulator (SOI) substrates with a starting thickness of 700 Å were used. Active regions were defined using LOCOS isolation. A poly-Si/SiO_2 (EOT ~30 Å) gate stack was subsequently formed, followed by liner oxide deposition. The lightly-doped drain extension is formed using a separate mask to cover the source region during implantation [Fig. 5(a)]. This is followed by the formation of the 1st nitride spacer, which also defined the I-region. Using the earlier implant mask, the heavily doped drain implant is performed. With another separate mask, the shallow source extension implant is carried out with the drain begin masked by photoresist. Next, a 2nd spacer is formed. This is followed by a deep source implant using the previous mask. Dopant activation is then performed (RTA 1000°C, 5 s), followed by contact and level-1 metallization. Structures with gate lengths (L_G) down to 60 nm were fabricated. Fig. 5(b) shows a TEM cross section of the DS I-MOS. The I-region has a length (L_I) of about ~40 nm.

4. RESULTS AND DISCUSSION

For device operation, the source is negatively biased with the drain at a positive bias. Thus, appropriate source bias should be determined, and the impact of drain/gate bias on V_{BD} is important. Fig. 6 depicts the breakdown characteristics of the DS I-MOS. Higher reverse-biased leakage current is observed at short L_G. The breakdown characteristic is also more abrupt, and tends to degrade at longer L_G. In addition, V_{BD} decreases with L_G (Fig. 7). All these phenomena could be explained by the resistance model of the gated p-i-n diode (inset of Fig. 7). At short L_G, the channel resistance R_{CH} is smaller and more voltage is dropped across the I-region (R_I). Thus, the leakage current is higher, and V_{BD} is lower. At longer L_G, the breakdown characteristics degrade as most of the increasing source voltage V_S is dropped across R_{CH}, and the change in electric field in the I-region is not as abrupt as in short L_G. Thus, the ratio between R_{CH} and R_I should not be too large, and should be in the range of 0.8-2.0. It is noted that R_{CH} is not simply a function of L_G as it is under the influence of the gate. Fig. 8 depicts how the gate influences the breakdown characteristics. With gate bias, the channel is under inversion, and R_{CH} drops by a substantial amount. This causes V_{BD} to drop by ~0.55 V. This is termed as gate-induced breakdown voltage lowering (GIBVL). The leakage current is also higher due to the shortening of the effective channel length.

DIBVL of ~0.25 V/V is also observed as the drain bias is varied (Fig. 9). Higher drain bias results in a slight reduction in R_{CH}, and higher band-to-band tunneling from the channel to drain. A summary plot of the DIBVL and GIBVL effect as a function of L_G is plotted in Fig. 10. Similar to the short channel effect in MOSFET, the DIBVL and GIBVL effect is more prominent at shorter L_G. Now, based on Fig. 8 and Fig. 9, to operate an I-MOS load inverter with an output swing from 0 V to 1 V, the source bias should be in the range of -5.6 V to -5.9 V. In this case, we select V_S to be -5.75 V. Fig. 11 shows the gate transfer characteristics of a 60 nm gate length DS I-MOS transistor. Excellent subthreshold swing of 11.7 mV/decade is achieved with ~4-5 orders of I_{on}/I_{off} ratio.

5. CONCLUSION

A double-spacer (DS) I-MOS transistor was fabricated and characterized. Process modifications were applied to optimize the device performance. The drain/gate bias effect on breakdown characteristics was studied and analyzed. This provides more insights to the device operation of the I-MOS, and the selection of the source voltage. Finally, excellent subthreshold swing and good device performance were achieved.

REFERENCES

[1] K. Gopalakrishnan *et al.*, *IEDM Tech. Dig.*, pp. 289-292, 2002.
[2] W. Y. Choi *et al.*, *IEDM Tech. Dig.*, pp. 203-206, 2004.
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[4] W. Y. Choi *et al.*, *TED.*, vol. 53, no. 5, pp. 1282-1285, 2006.

Table 1. Summary of the process modifications carried out in this work and the impact on device characteristics.

Process Modification	Impact
Lightly Doped Drain Extension Implant	Reduce the effect of drain bias on breakdown voltage
Heavily Doped Drain Implant	Reduce drain series resistance
Shallow Source Extension Implant	Reduce the breakdown voltage
Deep Source Implant	Reduce source series resistance

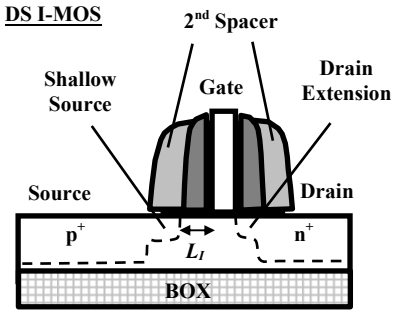

Fig. 3. Schematic of the Double Spacer (DS) I-MOS. Drain extension is lightly doped to reduce drain biasing effect on breakdown voltage and threshold voltage. The 2nd spacer is formed so that a shallow source implant could be employed to reduce the breakdown voltage.

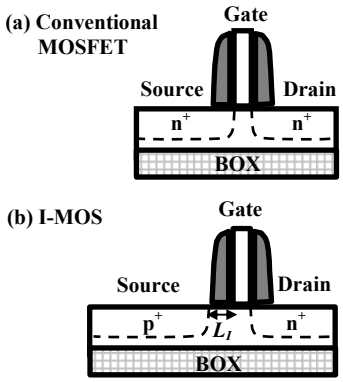

Fig. 1. Schematic of (a) conventional MOSFET, and (b) Impact-ionization MOS (I-MOS) transistor. For an n-channel I-MOS, the drain is doped n^+ while the source is doped p^+.

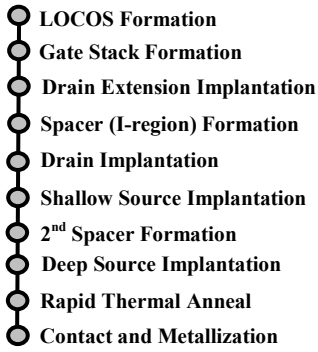

Fig. 4. Summary of important fabrication process steps for the formation of the DS I-MOS transistor. The 1st spacer is used to define the length of the I-region L_I, and photoresist is used to block the drain/source region when implantation is carried out on the source/drain region.

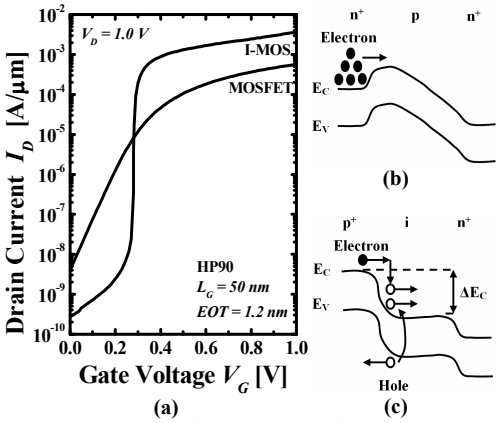

Fig. 2. (a) Simulated gate transfer characteristics for conventional MOSFET and I-MOS. (b) & (c) show their respective energy band diagrams and conduction mechanism in the on-state during device operation.

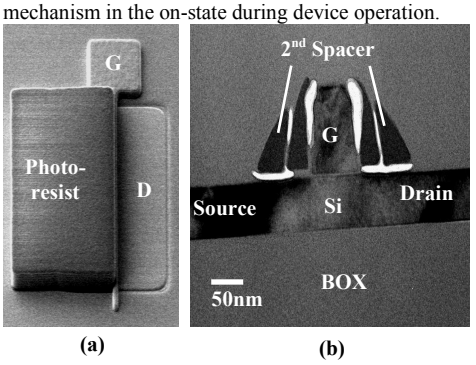

Fig. 5. (a) SEM view of fabricated I-MOS showing the source being covered by photoresist during drain extension implantation. (b) TEM picture of the DS I-MOS transistor showing the double-spacer. Cleaning steps have caused part of the liner oxide to be washed away.

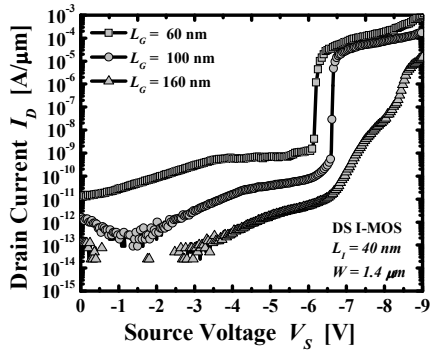

Fig. 6. Plot of measured I_D-V_S for DS I-MOS at various gate lengths. Higher reverse-biased leakage current is observed at shorter gate length.

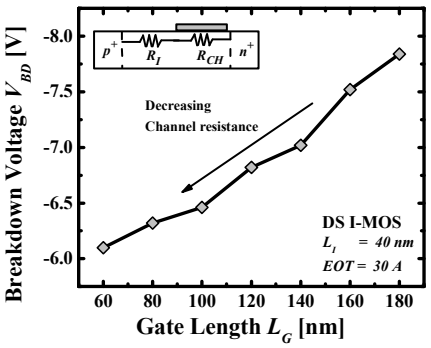

Fig. 7. The breakdown voltage decreases as the gate length decreases. This is a direct result of the reduction of channel resistance (inset) with gate length.

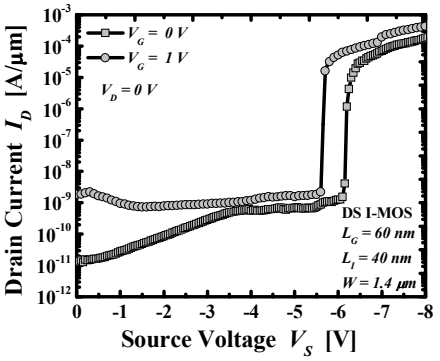

Fig. 8. Measured I_D-V_S for DS I-MOS at different gate biases. Increasing gate bias reduces the effective channel length and hence lowers the breakdown voltage.

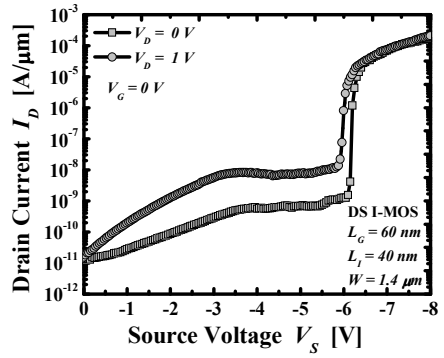

Fig. 9. Measured I_D-V_S for DS I-MOS at different drain biases. Increasing drain bias reduces the breakdown voltage and increases the band-to-band tunneling current from channel to drain.

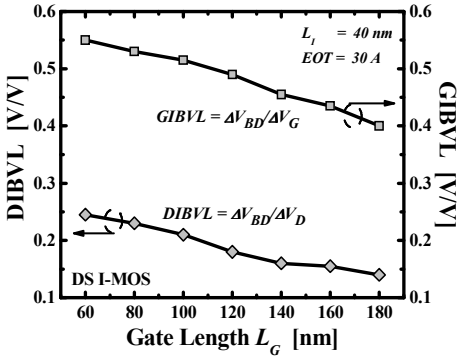

Fig. 10. The drain and gate bias has a greater effect on the changes in breakdown voltage at shorter gate length.

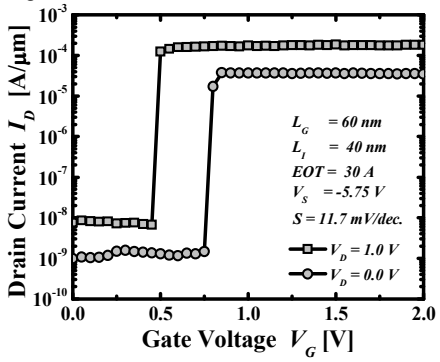

Fig. 11. Gate transfer characteristics for DS I-MOS at different drain biases. Excellent subthreshold swing of 11.7 mV/decade is achieved.