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Identification of Single and Coupled Acceptors in Silicon Nano Field-Effect Transistors

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1. Introduction

Single-dopant electronics, in which we exploit the dopants (or "true atoms") instead of quantum dots (or artificial atoms) in order to manipulate the electronic charges and spins, could be a key for future nano/quantum information technology. In the present early stage of the research in this field [1-3], it is crucial to identify individual dopants in a FET as a first step.

Here, we investigate the low-temperature current characteristics of nano FETs containing only up to a few boron acceptors with the aim of determining the acceptor location (depth) and of observing the coupling between two acceptors.

2. Device Structure and Measurements

Nano FETs, shown schematically in Fig. 1, were fabricated on a SOI substrate. They have a $p^+/p/p^+$ structure and two-layered (upper and front) gate. Owing to this two-layered gate, it is possible to investigate the effect of channel dopants (boron) on the current without the annoyance of dopant diffusion from the heavily doped source and drain. The channel doping concentration was estimated to be 1.9×10^{16} cm^{-3} [3], which indicates that the average number of boron acceptors under the front gate is around 1 or 2.

We measured the drain current (I_D) while sweeping the front-gate voltage (V_F) and stepping the back-gate voltage (V_B) in a 0.25 V interval at fixed upper gate voltage $V_U = -5$ V. A negative V_U generates a hole accumulation layer around the front channel, which acts as the electrically induced leads for the front-gate nano FET. All measurements were performed at 6 K.

3. Results and Discussion

We first discuss the characteristics for an undoped FET, in Fig. 2. As shown in Fig. 2(b), the amount of the current-curve shift is not equal between the positive and negative V_B sides, as denoted by Δ_{LF} and Δ_{LB}. This change in the interval reflects the depth of the hole channel in the SOI, and a sufficiently large positive (negative) V_B makes it possible to identify the channel as the front (back) one [4]. In the gray-scale plot of $d(\mathrm{Log}|I_D|)/dV_F$ shown in Fig. 2(a), the threshold voltage is indicated by solid and dotted white lines for the back and front channel, respectively. The belt coloured in black corresponds to the subthreshold region because $d(\mathrm{Log}|I_D|)/dV_F$ [$= (d|I_D|/dV_F)/|I_D|$] has a large negative value there.

Figures 3, 4, and 5 show the results for three different samples of doped FETs. Different from the undoped sample (Fig. 2), we observe a current modulation, which is ascribed to the charging effect on a single acceptor [3]. In fact, as shown in Fig. 6, the Coulomb diamond was observed in the differential conductance characteristics.

We hereafter discuss each sample in detail. In Fig. 3(b), there are two series of current modulations, one with rapidly increasing $|I_D|$ with increasing V_B, and the other showing "U-shaped" dependence of $|I_D|$ on V_B [seen in the upper-left corner of Fig. 3(b)]. We expect that each modulation comes from one of two different acceptors.

Focusing on the first type, we see this modulation as a white curve, marked by arrows 1, 2, and 3, running across the subthreshold black belt in Fig. 3(a). Because the slope (i.e. dV_B/dV_F) is determined by the coupling ratio of the capacitances to the front and back gates, it should convey information about the acceptor depth. Near arrow 1, the slope of the bright curve is close to that of the back-channel threshold-voltage line (solid white line), which strongly suggests that the acceptor is located near the back interface. As V_F is decreased, the slope decreases, especially when the channel moves to the front side (around arrow 3). This reduced slope can be explained by the shielding of the electrical flux from the front gate due to the emergence of the front channel between the front gate and the acceptor site. The situation appears to be completely opposite for the FET in Fig. 4, from which the location of the corresponding acceptor is ascribed to the region near the opposite interface, the front one.

In Fig. 5(a), we observe the third "pattern", in which the slope increases and decreases when we apply a larger positive and negative V_F, respectively. We ascribe this third pattern to the acceptor located around the middle of the SOI. In such a case, the current exhibits the U-shaped structure as shown in Fig. 5(b). We show in Fig. 7 the simplified potential diagrams explaining the above-mentioned samples.

Going back to Fig. 3, two series of current modulations, which are expected to originate from two different acceptors, cross at around $V_B = 5$ V. Noticeably, the capacitive coupling between these two acceptors is observed [see white and black circles near arrow 3 in Fig. 3(a)]. This is the first observation of coupling of acceptors in silicon FETs and could be a good experimental host for investigating the charge shuttling between dopant atoms.

4. Conclusions

In a transport experiment we were able to access the depth of each dopant in a SOI FET. We also showed data that support the coupling of two acceptors in a FET.

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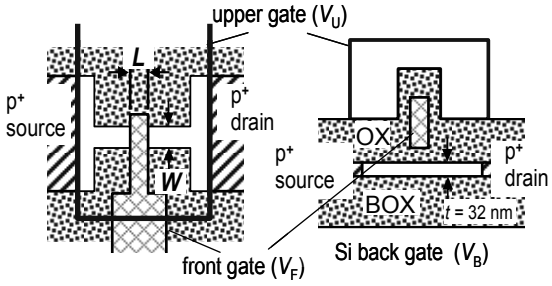

Fig. 1. Schematic top (left) and cross-sectional (right) views of a nano-FET. The SOI thickness is 32 nm. OX and BOX are the gate oxide and buried oxide, respectively. The front-gate length (L) is 40 nm and the width (W) is 40 nm or 70 nm.

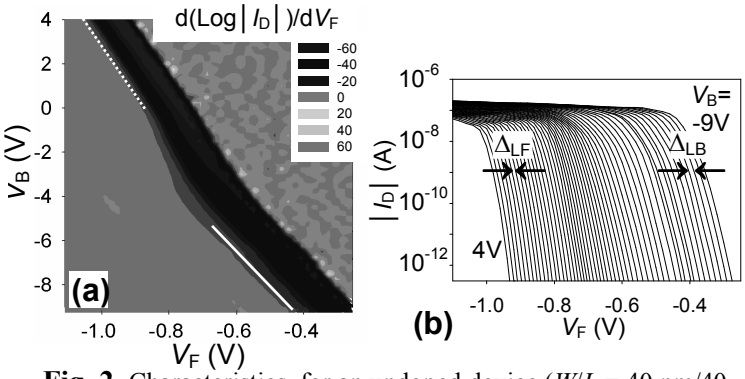

Fig. 2. Characteristics, for an undoped device (W/L = 40 nm/40 nm) measured at drain voltage V_D = -10 mV, of (a) d(Log $|I_D|$)/dV_F vs. V_F-V_B and (b) $|I_D|$ vs. V_F for various V_B. Solid and dotted white lines in (a) are the back and front channel threshold voltages, respectively.

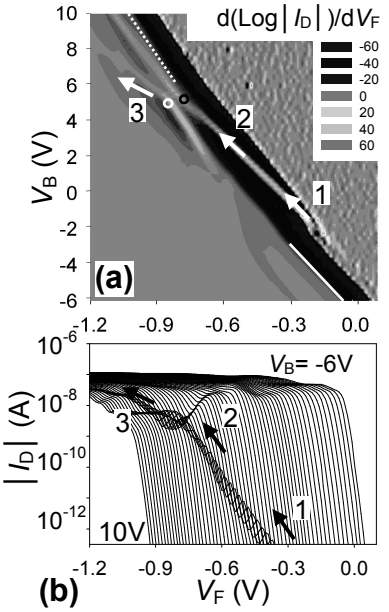

Fig. 3. Characteristics, for a doped device (W/L = 40 nm/40 nm) measured at V_D = -10 mV, of (a) d(Log $|I_D|$)/dV_F vs. V_F-V_B and (b) $|I_D|$ vs. V_F for various V_B.

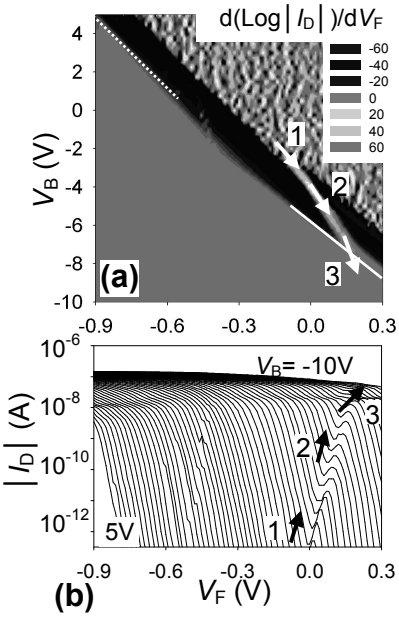

Fig. 4. Characteristics, for a doped device (W/L = 70 nm/40 nm) measured at V_D = -10 mV, of (a) d(Log $|I_D|$)/dV_F vs. V_F-V_B and (b) $|I_D|$ vs. V_F for various V_B.

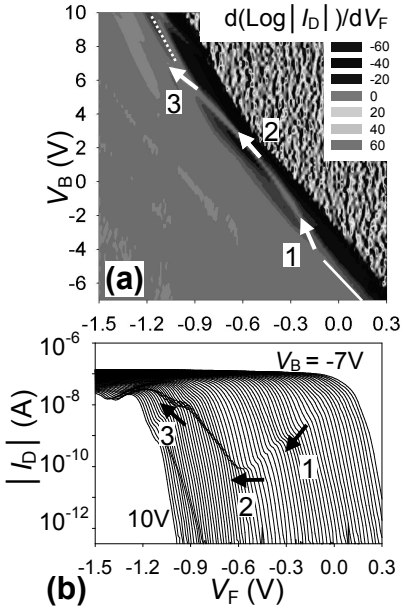

Fig. 5. Characteristics, for a doped device (W/L = 70 nm/40 nm) measured at V_D = -10 mV, of (a) d(Log $|I_D|$)/dV_F vs. V_F-V_B and (b) $|I_D|$ vs. V_F for various V_B.

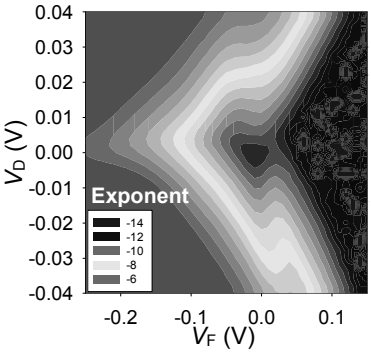

Fig. 6. The differential conductance dI_D/dV_D vs. V_F-V_D measured at V_B = -4 V for the FET shown in Fig. 4. Only one diamond is observed, showing that the acceptor captures one hole.

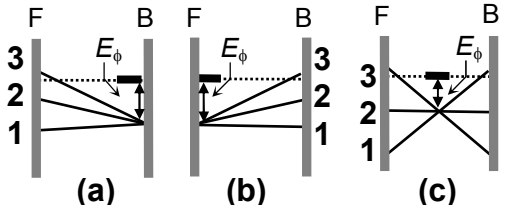

Fig. 7(a), (b) and **(c).** Band diagrams at the peak positions 1, 2, and 3 in Figs. 3, 4, and 5, respectively. The solid line, dotted line, and small bar are respectively the valence band edge, Fermi level, and acceptor level between the front (F) and back (B) interfaces. The acceptor ionization energy is defined as E_ϕ.