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Self-Aligned Dual-Gate Single-Electron Transistors (DG-SETs)

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1. Introduction

Single-Electron Transistors (SETs) are actively being studied as an alternative or supplement to CMOS technology beyond the point when CMOS is predicted to face critical scaling limits. Although SETs can offer high effective integration density, low power operation and high functionality, it has drawbacks which can be solved by utilizing the dualistic character of MOSFETs. This necessitates the co-integration of SETs and MOSFETs on a single substrate, which consequently requires the fabrication of SETs on Si substrates with a process sequence similar to that of MOSFETs. Such discussion has brought about extensive research in the field of silicon-based SETs [1]. Of these methods, some make use of uncontrollable fabrication methods, eliminating the possibility of its practical usage. Others such as Dual-Gate(DG) SETs utilize a more controllable and reliable one [2]. The latter comprehends the above-mentioned requirements for the realization of SETs, meaning the search for its improvements is justified. In this paper, we present a self-aligned DG-SET showing enhanced process compatibility with conventional MOSFETs, while at the same time overcoming the problems that were persistent in the previously reported fabrication methods.

2. Previous work

Several CMOS process based fabrication methods for DG-SETs have previously been introduced [2-4]. However, the fabrication process was somewhat dissimilar to conventional MOSFET process, and moreover, inherent parasitic MOSFET components caused the device to cut-off at low control gate voltages, and the MOSFET current to overwhelm the SET current at high voltages, consequently degrading the Peak-to-Valley Current Ratio (PVCR) of the device. Taking such issues into consideration, the structure shown in Fig. 1(b) is proposed as a solution. The simulated conduction band edge diagram for the previous device and the self-aligned device are presented in Figs. 2(a) and (b), respectively. It can be noted that for the self-aligned structure, the electrically induced tunneling barriers remain constant even when the control gate voltage is increased to a high level. Since the MOSFET current domination at high control gate voltages is caused by energetic electrons that have energies exceeding the height of the tunneling barrier, it can be noted that in the case of the newly proposed device, the degradation of the PVCR can be greatly reduced.

3. Device Fabrication

The devices were fabricated on a p-type (100) SOI wafer. SOI thickness was reduced to 28 nm from an initial thickness of 300 nm, through a series of thermal oxidation and subsequent oxide wet etch step. The active region was defined through a mix-and-match of photo/e-beam lithography, and subsequent silicon plasma etch process. The minimum width of the active was around 30 nm. A cross-sectional SEM image of an active test pattern is shown in Fig. 3(a). Afterwards, a 145 Å control gate oxide was formed through dry thermal oxidation. This, at the same time reduced the width and height of the SOI active by 13 and 7 nm, respectively. Then the gate a-Si layer was deposited by means of LPCVD and patterned through e-beam lithography. The gate a-Si and control gate oxide was etched by a plasma etch process. The minimum gate length at this point was 40 nm. Through a thermal dry oxidation step, the side gate oxide layer and inter-gate isolation oxide layer was formed simultaneously. Due to the combined effects of etch undercut during the gate a-Si etch process and silicon consumption during the oxidation process, the gate length was reduced by approximately 25 nm and the SOI thickness by 50 Å. Afterwards, in order to form the sidewall spacer gates along the control gate, an a-Si layer was deposited through LPCVD and etched back by plasma etch processing. Implant offset TEOS sidewall spacers were formed along the side gates, which was followed by source/drain implantation. A cross-sectional SEM image of a test pattern of the gate side is shown in Fig 3(b).

4. Results and Discussion

The whole fabrication process is highly compatible with the conventional CMOS process. Moreover, the process sequence is actually identical to virtual source/drain type MOSFETs [6]. This implies that the self-aligned DG-SET can be readily co-integrated with MOSFETs, making the integration of various CMOS-SET hybrid circuit applications that have previously been suggested possible [7]. Another merit is that the total capacitance of the dot, which determines the operation temperature of the device, can be decreased beyond the limit posed by lithography by means of thermal oxidation. This was taken into account in the main device fabrication. The room temperature transfer characteristic of the fabricated device is as shown in Fig. 4. Although no oscillation peaks and valleys are visible in the

current curve, the trans-conductance curve shows two clear peaks, indicating single-electron tunneling operation of the proposed device.

5. Conclusions

A new self-aligned Dual-Gate Single-Electron Transistor (DG-SET) with high process compatibility with MOSFET and the potential of suppressing parasitic effects shown in previous structures was proposed. Such effects were verified through simulation. A fabrication sequence was proposed and the device fabrication was carried out. Room temperature measurement of the transfer characteristic revealed a double peak in the trans-conductance curve proving the single-electron tunneling operation of the device.

Acknowledgements

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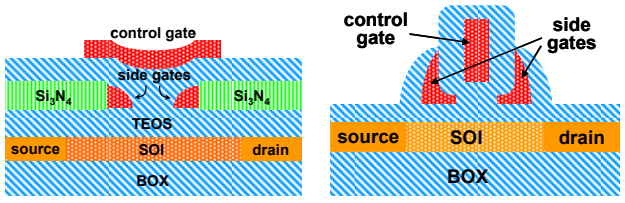
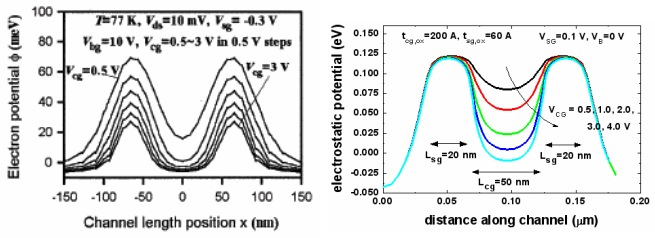


(a) (b)

Fig. 1 Structural depiction of the (a) previous and (b) self-aligned version of the DG-SET.



(a) (b)

Fig. 2 Simulation results of the electrostatic potential formation along the channel for the (a) previous DG-SET and the (b) self-aligned DG-SET.

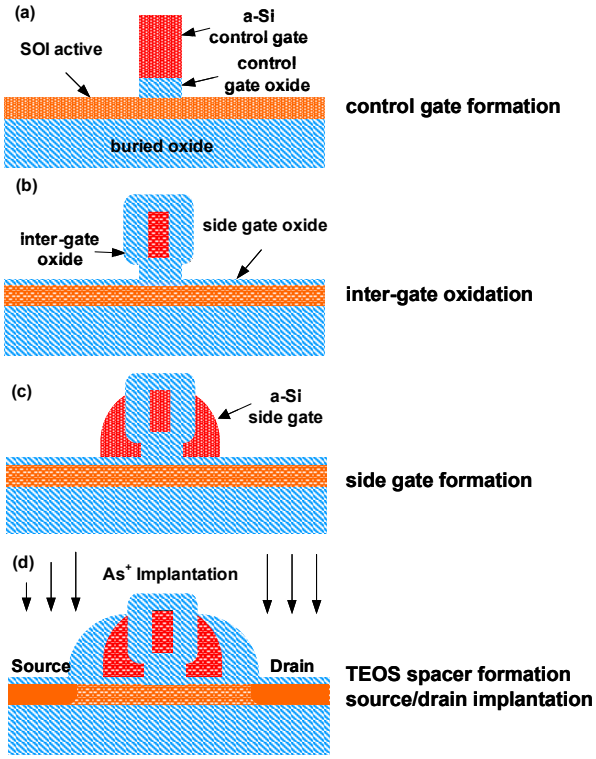
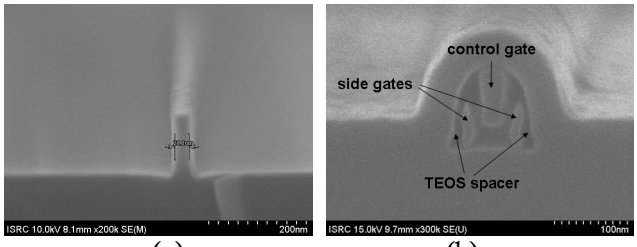


Fig. 3 Fabrication process flow of the self-aligned DG-SET.



(a) (b)

Fig. 4 Cross-sectional SEM image of the test patterns for the (a) active side after Si-etch and of (b) the gate side. The gate side view was prepared by an additional poly-Si deposition and oxide staining process by means of HF dipping.

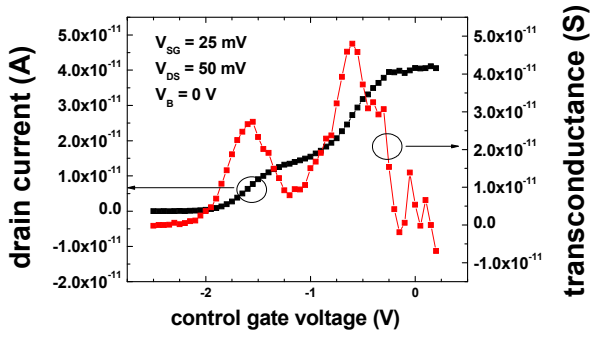


Fig. 5. Room temperature trasnfer characeteristic of the self-aligned DG-SET. Device parameters for the device are L_{cg} = 15 nm, L_{sg} = 45 nm, W = 10 nm, $t_{ox,cg}$ = 350 Å, $t_{ox,sg}$ = 120 Å.