Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 1138-1139

I-10-4

Design Control of Random Dopant-induced Multiple-Tunnel-Junction Arrays for Turnstile Operation

D. Moraru, K. Yokoi, H. Ikeda, and M. Tabe
Research Institute of Electronics, Shizuoka University, 3-5-1 Johoku, Hamamatsu 432-8011, Japan
Phone/Fax: +81-53-478-1335 E-mail: daniel@rie.shizuoka.ac.jp

1. Introduction

As device dimensions are scaled down towards 10 nm, discrete distribution of dopant impurities strongly affects the device electrical properties [1]. We have recently demonstrated that a phosphorous (P)-doped Si-nanowire field-effect transistor (FET) exhibits turnstile operation, i.e., an electron is correctly transferred from the source to the drain by a cycle of ac-gate voltage [2]. It should be noted that in this device randomly distributed P ions work as Coulomb dots, leading to the formation of a multiple-tunnel-junction (MTJ) single-electron transistor (SET) [3]. The schematic top view of this FET is depicted in Fig. 1(a). The Si nanowire, including some P ions indicated by black points, is placed between source and drain electrodes, and one top gate overlies the channel (not shown). Figure 1(b) shows the experimental results of the drain current (I_d) for both dc- and ac-gate operation as a function of drain voltage (V_d) at 5.5 K. Under ac-gate operation, the I_d-V_d curve exhibits small plateaus aligned around $\pm ef$ current levels (f=1 MHz in this case), which indicates turnstile operation. Although it was surprising that such random MTJ-FETs allow turnstile operation, we have found by simulation that it is possible when parameters as junction and gate capacitances are set in appropriate ranges.

However, since the positions of P atoms are random and uncontrollable, even if we know that the FETs work as turnstile devices with high probabilities, we cannot control with certainty the turnstile operation. Thus, one question naturally arises: Is there any way to design and control devices to exhibit turnstile operation utilizing randomly distributed P ions? In this paper, we propose a way to control the potential profile by a statistically attained method, i.e., by designing the macroscopic channel shape, as illustrated in Fig. 1(c). For this purpose, at first, we numerically investigated ac I_d-V_d characteristics for various 1D MTJ arrays with different distributions of dot-gate capacitances C_g and we clarified the arrangements most favorable for turnstile operation. Then, in correlation with these favorable 1D arrangements, we investigate 2D MTJ arrays in which the C_g's in the 1D case are replaced by several dots in parallel. Turnstile operation is consistently reproduced, suggesting that the microscopic randomness of dopant positions could be macroscopically controlled by an appropriate channel design.

2. Turnstile operation in 1D MTJ arrays

Figures 2(a)-(d) show typical equivalent circuits for 1D MTJ arrays (junction capacitance C_j=0.2 aF and resistance R_j=0.1 MΩ) containing 3 quantum dots (shown by dashed circles). In this study, we consider parameter randomness by introducing dispersion in the gate capacitances of the dots (C_{gi}=0.5-1.5 aF; i=1-3). Since the gate electrode overlies the channel, all dots are simultaneously biased by the gate voltage (V_g) through each C_{gi} (omitted in the figure for simplicity). We calculate the I_d for each circuit by employing a Monte Carlo method based on the Coulomb blockade orthodox theory. The calculation procedure was the same as in our previous work [4].

The sizes of the dashed circles in Fig. 2 correspond to the dot gate capacitances. For instance, the MTJ array in Fig. 2(a) has the relationship $C_{g2}>C_{g1}>C_{g3}$. Hereafter, we denote the capacitance arrangement like this array with M-L-S, i.e., medium-large-small values for C_{gi}. In this case, as well as for the S-L-S array in Fig. 2 (b), it is clearly found that the calculated I_d-V_d curves exhibit plateaus at $+nef$ levels, meaning that turnstile operation is achieved. On the other hand, an L-S-L MTJ array ($C_{g1}=C_{g3}>C_{g2}$), as shown in Fig. 2(c), does not show the turnstile operation. From the I_d-V_d characteristics calculated for 130 various capacitance arrangements, we statistically found that about 50% of the S-L-S and M-L-S arrays investigated exhibit turnstile operation. In contrast, L-S-L and S-M-L arrays hardly ever show turnstile features. These facts indicate that there are some capacitance arrangements favorable for the turnstile operation.

3. Application to 2D MTJ arrays

The analysis has been then extended to 2D MTJ arrays in analogy with the 1D case. For the 2D case, all dots have uniform gate capacitances C_{gi}=0.5 aF. Dots with larger C_{gi} in 1D arrays are replaced with several parallel dots in the 2D arrays. Figures 3(a)-(d) show typical equivalent circuits of 2D MTJ arrays, corresponding to the 1D arrays shown in Fig. 2, and their calculated ac I_d-V_d characteristics. It can be clearly seen that the $+nef$ plateaus are reproduced again for the cases of the S-L-S and M-L-S arrays, but not for the L-S-L and S-M-L cases. These results strongly suggest that we can achieve turnstile operation by a macroscopic design control over the random dopant-induced MTJ arrays.

4. Conclusions

We numerically investigated I_d-V_d characteristics under ac-gate voltage for 1D and 2D MTJ-FETs and found that turnstile operation is often observed when the center dot has larger C_{gi}, which corresponds to a doped channel wider at the center. These results enable us to fabricate single-gated MTJ-FETs for turnstile operation simply by appropriately designing the doped channel shape.

This work was partly supported by MEXT KAKENHI (18063010 and 16106006).

References

[1] S. Roy and A. Asenov, Science **309** (2005) 388.
[2] D. Moraru, Y. Ono, H. Inokawa, K. Yokoi, R. Nuryadi, H. Ikeda, and M. Tabe, Ext. Abstr. SSDM (2006) 820.
[3] G. J. Evans, H. Mizuta, and H. Ahmed, Jpn. J. Appl. Phys. **40** (2001) 5837.
[4] H. Ikeda and M. Tabe, J. Appl. Phys. **99** (2006) 073705.

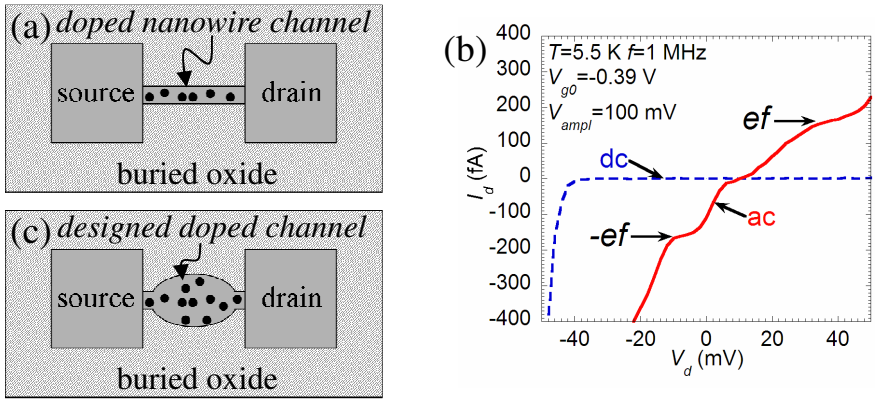

Fig. 1 (a) Schematic top-view of doped nanowire FET as experimentally investigated. (b) Experimental dc (dashed curve) and ac (solid curve) I_d-V_d characteristics. Current plateaus aligned at $\pm ef$ levels can be observed indicating turnstile operation. (c) Channel design possibly favorable for turnstile operation.

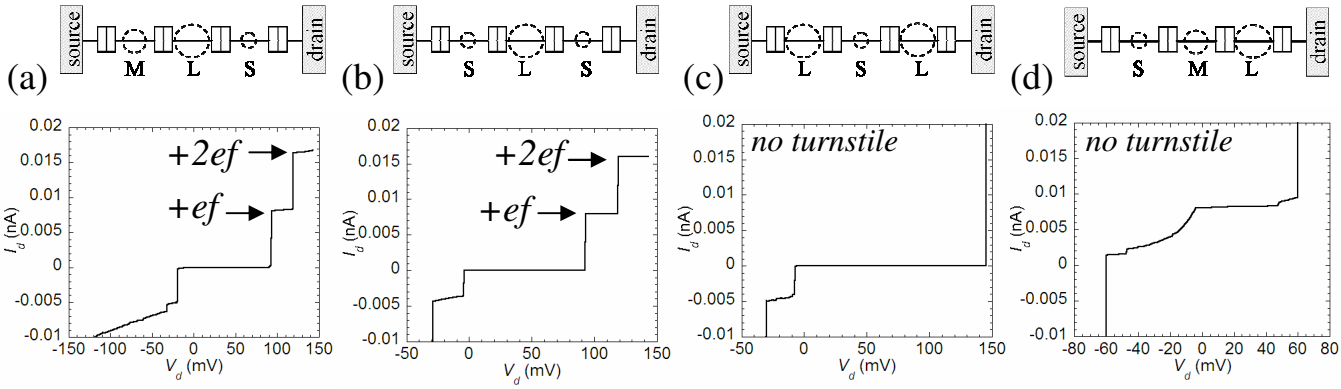

Fig. 2 Equivalent circuits and simulated ac I_d-V_d characteristics for 1D MTJ arrays with various C_g arrangements. Dots symbolized by dashed circles have different gate C_g, as indicated also by the indexes S (small), M (medium), and L (large), respectively. In (a) M-L-S and (b) S-L-S arrays, turnstile operation is achieved (as indicated by arrows), but not in (c) L-S-L and (d) S-M-L arrays.

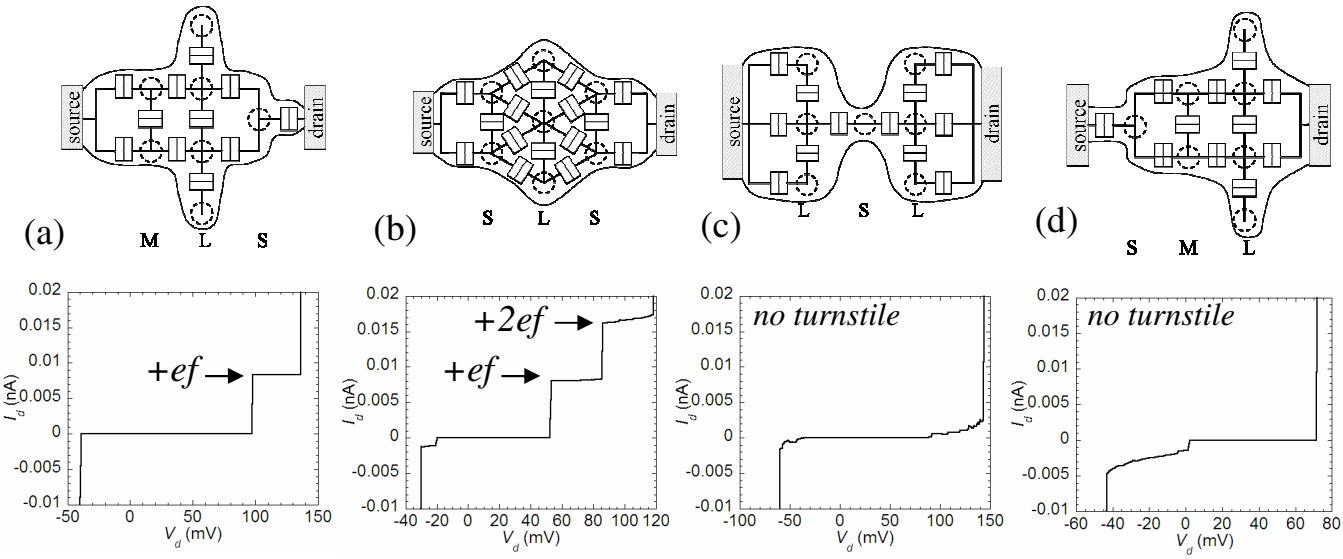

Fig. 3 Equivalent circuits and simulated ac I_d-V_d characteristics for 2D MTJ arrays with various C_g arrangements. The cases correspond to those in Fig. 2, but dots with larger C_g have been replaced with several dots in parallel as in more realistic 2D devices. Turnstile operation (indicated by arrows) is observed for (a) M-L-S and (b) S-L-S, but nor for (c) L-S-L and (d) S-M-L arrays, consistent to 1D case.