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Room Temperature Oscillation in $Si/Si_{1-x}Ge_x$ Resonant Tunneling Diode

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1. Introduction

$Si/Si_{1-x}Ge_x$ resonant tunneling diodes (RTDs) have been intensively studied as one of next-generation quantum effect devices formed with Si-system materials. However, their oscillations have not been reported at any temperature yet.

We have so far applied a combination of electron tunneling and double quantum well (DQW) using the type II band offset [1-5], and have reported high PVCRs of >180 at RT [2-5]. To form the type II hetero structure, a strain-relaxed SiGe buffer should be first formed on a Si substrate. For the buffer, a thick $Si_{1-x}Ge_x$ graded buffer, where the Ge composition, x, is varied by 0.1 μm^{-1}, is commonly used [6]. To save the production energy and time, we have previously proposed a thin triple-SiGe-layer (TL) [3,4] and a thin quadruple-SiGe-layer (QL) [5] buffer. Each thickness is about one-fifteenth of that of the graded buffer. Especially, the QL buffer also exhibits high surface crystallinity even when it is highly P-doped to increase the current density.

In this paper, we first report the observation of oscillation in a $Si/Si_{1-x}Ge_x$ RTD at room temperature (RT). The RTD has an electron-tunneling type-II DQW structure and is formed with a highly P-doped QL buffer.

2. Experimental

Si and $Si_{1-x}Ge_x$ layers were grown on 0.01 Ωcm n-type Si(001) at a substrate temperature of 600 ºC by gas-source molecular beam epitaxy in a vacuum chamber with a base pressure of $< 1\times10^{-9}$ Torr using Si_2H_6, GeH_4 and PH_3 for Si, Ge, and P dopant gas sources, respectively.

3. Results and Discussion

3.1 Strain-relaxed doped quadruple-layer (QL) buffer

In the case of the TL buffer (Fig. 1(a)) [3,4], the first and second SiGe layers are grown almost coherently, and when the top (third) SiGe layer is grown, misfit dislocations are mainly generated in the lowest interface and the buffer relaxes. The top SiGe layer prevents the threading dislocations from being propagated to the top layer. The surface threading dislocation density, D_T is low as indicated in Fig. 2(a). However, when the TL buffer is highly doped with P to increase the current density, the buffer surface crystallinity degrades and the D_T increases by a factor of 1000 as shown in Fig. 2(b).

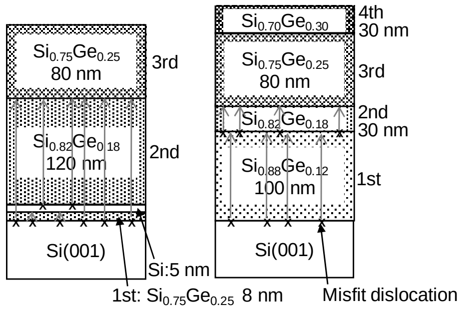

Fig. 1. Our proposed thin triple-SiGe-layer (TL) and thin quadruple-SiGe-layer (QL) strain-relaxed buffers.

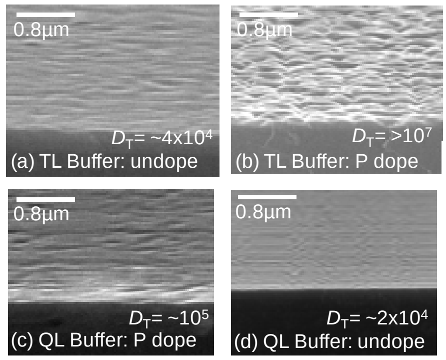

Fig. 2. Scanning electron microscope images obtained from (a) an undoped TL, (b) a doped TL, (c) a doped QL, (d) an undoped QL buffer. Each threading dislocation density, D_T (cm^{-2}), is also indicated.

To prevent this crystallinity degradation, we have proposed the QL buffer where the buffer is designed so that the misfit dislocations are evenly distributed in the lower two interfaces (Fig. 1(b)) [5]. Due to this dislocation distribution, the QL buffer surface crystallinity remains well even when it is highly doped (Figs. 2(c), (d)). The two top layers drive the buffer relaxation and also prevent the threading dislocations from being propagated to the top layers (Fig. 1).

3.2 $Si/Si_{1-x}Ge_x$ RTD and its room-temperature oscillation

Using the highly P-doped QL buffer with a high crystalline surface, electron tunneling symmetrical DQW RTD was fabricated on a 0.01 Ωcm n-type Si(001) substrate as shown in Fig. 3. The undoped double-well part is sandwiched by 10-nm undoped Si. The doping densities of the n-type layers were all $\sim4\times10^{18}$ cm^{-3}.

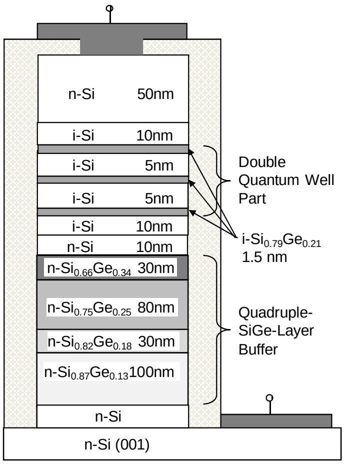

Fig. 3. The structure of fabricated symmetrical double quantum well (DQW) RTDs.

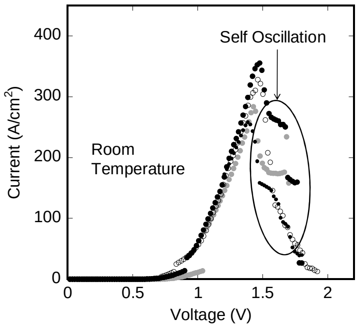

Fig. 4. Typical *I-V* curves obtained from a DQW RTD with a diameter of 25 μm at RT. Self Oscillations were observed.

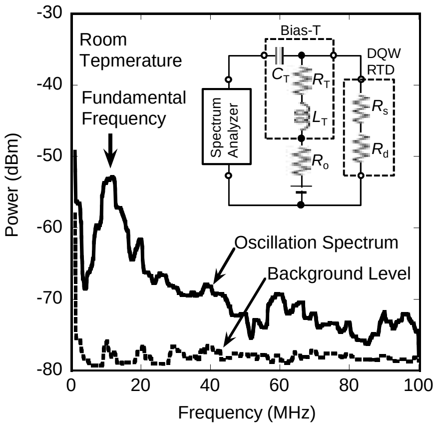

Fig. 5. Oscillation spectrum obtained from a DQW RTD with a diameter of 15 μm at RT. The measurement circuit is indicated in the figure.

Typical *I-V* curves obtained from a DQW RTD with a diameter of 25 μm at RT are shown in Fig. 4. Self oscillations were observed in the *I-V* curves at ~1.7 V at RT.

We have also first observed oscillation in the DQW RTD with a diameter of 15 μm at RT using a bias-T. We show the oscillation spectrum in Fig. 5. The measurement circuit is indicated in the figure. The DC source has an output resistance, R_0, of 50 Ω. The bias-T consists of R_T (9 Ω), C_T (96 nF), and L_T (1.5 mH). The oscillation frequency was 11 MHz. The static *I-V* curve shows that the resonant peak

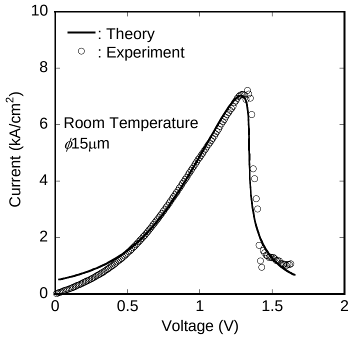

Fig. 6. *I-V* curve obtained from the DQW RTD exhibiting oscillation at RT and theoretical fitting curve

current is as high as ~7.2 kA/cm^2 as shown in Fig. 6. The oscillation was generated just in the negative differential resistance (NDR) region. A theoretical curve can be fitted to the experimental data using Lorentzian functions for the quantized states in the double well and a thermionic emission function considering series resistance R_s (Fig. 6). From this curve fitting, the R_s and the NDR, R_d values are estimated to be 30 and -30 to -200 Ω, respectively. At the oscillation frequency, the $R_s + R_d$ is estimated to be -125 Ω which corresponds to the *I-V* curve fitting results. The maximum oscillation frequency is also estimated to be ~3 GHz using the theoretical equation [7]. Thus, the observed frequency was limited by the bias-T circuit parameters. The average number of the surface threading dislocations of the RTD is less than 1 estimated from the D_T value indicated in Fig. 2(c). The oscillation generation may be connected with the low defect density in addition to the high resonant peak current density.

4. Conclusions

We fabricated an electron-tunneling $Si/Si_{1-x}Ge_x$ DQW RTD using the previously proposed highly P-doped quadruple-layer buffer with a high crystalline surface. The average number of the buffer surface threading dislocations is < 1. The RTD shows a good resonance curve and a high peak current density. We have first observed oscillation in the $Si/Si_{1-x}Ge_x$ RTD at RT. The oscillation frequency was limited by the measurement circuit and was 11 MHz. The estimated max frequency, f_{max}, is ~3 GHz. The f_{max} will increase by the reduction in the series resistance, R_s. The $Si/Si_{1-x}Ge_x$ RTD technology is expected to evolve by our room-temperature oscillation observation result.

References

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