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Effect of Size Reduction on Operation Temperature and Switching Power in GaAs-Based Schottky-Wrap-Gate Quantum Wire Transistors

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1. Introduction

The charge-control-type quantum nano-devices such as quantum wire transistors (QWRTrs) and single electron transistor (SET) have possibility to operate with ultra low power consumption near the quantum limit defined by the Heisenberg's uncertainty. Our research group proposed and has developed a novel ultra-low-power logic circuit integrating QWRTrs and SETs as ultra-low-power path-switches for a few electrons [1] In this circuit, switching power of QWRTrs and SETs directly reflects on the system power performance. However, few systematic studies have been made on minimizing their power consumption as well as increasing operation temperature yet.

The purpose of this paper is to investigate the effects of feature size reduction on operation temperature and switching power consumption in Schottky wrap gate-controlled GaAs QWRTrs, through fabrication and characterization of devices with systematic size control.

2. Experimental

The device structure is schematically shown in **Fig. 1(a)**. It has a GaAs-based nanowire made of an AlGaAs/GaAs HEMT structure with a nanometer-scale Schottky wrap gate (WPG). Applying suitable gate voltage, V_G, the channel under the WPG is squeezed electrostatically and a quantum wire is formed. In a quantum transport regime, a few electron switching can be performed using the 1st step of quantized conductance as shown in **Fig. 1(b)**. The WPG structure is suitable for planar integration because of a simple lateral structure and precise size and position control utilizing the top-down fabrication process. Its high gate controllability by three-dimensional (3D) gate configuration and excellent transport of 2DEG in the AlGaAs/GaAs heterointerface are important in low switching power consumption.

GaAs-based nanowires were formed by EB lithography and wet etching of an AlGaAs/GaAs heterostructure wafer. Au/Cr Schottky WPGs were formed by the EB lithography, vacuum deposition and lift-off process. 2DEG mobility and carrier density of the wafer at 77 K were 1.1×10^5 cm^2/Vs and 1.0×10^{12} cm^{-2}, respectively. Electron mean free path at 77 K was 1.8 μm. Geometrical wire width, W, and gate length, L_G, were systematically changed as W=100~250 nm at 50nm intervals and L_G=100~800 nm at 100nm intervals.

Fabricated devices were characterized by I-V measurement in a low-temperature probe station using a standard semiconductor parameter analyzer. In this study, we focused on operation temperature and gate voltage-to-energy scaling factor, α. This directly relates to switching voltage, ΔV_{G0}, by the next formula, [2]

$$\Delta V_{G0} = 4kT/e\alpha. \quad (1)$$

Small ΔV_{G0} and large α need for low power switching, since switching energy is given by,

$$E_{sw} = C_G \Delta V_{G0}^2 = C_G(4kT/e\alpha)^2, \quad (2)$$

where C_G is gate capacitance. Existence of conductance quantization was judged from oscillation in differential conductance. The scaling factor and switching voltage were evaluated from the slope at the first conductance step. 3D potential simulation was also carried out for evaluating device parameters theoretically.

3. Result and Discussion

A SEM image of the fabricated WPG QWRTr is shown in **Fig. 2**. Nanowires were fabricated along <110> direction and trapezoidal cross sections with smooth (111)B side facets were realized. Geometrical sizes of fabricated devices were measured using the SEM.

An example of measured conductance is shown in **Fig. 3**. In this device, W=200 nm and L_G=500 nm. Three clear conductance steps were observed even at 100K. This is the highest temperature in previously reported III-V semiconductor-based QWRTrs.[3-5] Subband spacing by lateral confinement, ΔE, was estimated 30 meV, assuming $\Delta E \sim 3kT$. As shown in this example, reduction of geometrical wire width was effective for increasing operation temperature.

Experimentally obtained W and L_G dependence of the appearance rate of conductance quantization at 30K is summarized in **Fig. 4**. Here, the date was taken from 432 devices. In the case of $W \leq 300$ nm, 14 devices were measured for each element of the matrix in **Fig. 4**. The rate of conductance quantization strongly depended on W, but not on L_G. Decreasing W, the rate increased and high appearance rate of 80 % or more was obtained when $W \leq$ 300 nm. From the 3D potential simulation, it was found that confinement potential became steeper and stronger lateral confinement was formed by decreasing the geometrical wire width, rather than by decreasing the effective wire width electro-statically with decreased gate voltage. The reason of small influence of L_G was that

fabricated L_G was shorter than the mean free path.

Measured size dependence of V_G-to-E_F scaling factor, α, at 30 K is summarized in **Fig. 5**. α is defined by dE_F/dV_G and is less than 1. We evaluated α from ΔV_{G0} using **Eq. (1)**. Fabricated devices showed α of 0.2~0.3 and no clear W and L_G dependences were observed. We also evaluated the size dependence of α using the 3D potential simulation. The results are also plotted in **Fig. 5** by solid curves. The theory indicated that α increased by decreasing W. However, it remained in 0.2~0.3 when L_G>300 nm. These values roughly corresponded to the experimental ones. Then, disappear of the W dependence of α in the experimental data seemed due to the scattering of the data. When L_G< 300 nm, the theory indicated that α degraded as decreasing L_G, due to the short channel effect. However, experimental data hardly changed even when L_G<300 nm. This was understood by the effective gate length extension due to surface state charging in the gate periphery.[6] From the results, reduction of W less than 100 nm is difficult at present because gate threshold voltage exceeds Schottky barrier height. Then, a possible approach for further reduction of the power consumption is to decrease C_G by decreasing L_G with keeping the short channel effect small.

4. Conclusion

Size dependence of operation temperature and V_G-to-E_F scaling factor, α, in WPG QWRTrs was investigated by systematically changing W and L_G. Decreasing W, we could observe clear conductance quantization even at 100K. More than 80 % fabricated devices showed conductance quanti-zation at 30 K when W<300 nm. α=0.2~0.3 was obtained, which could be reproduced by the theory. It is still possible to decrease power consumption by decreasing gate capacitance with shorter gate length in the WPG QWRTrs.

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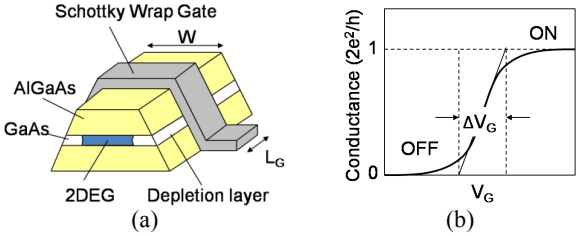

Fig. 1 (a) Basic structure of WPG QWRTr and (b) switching operation in 1D quantum transport domain.

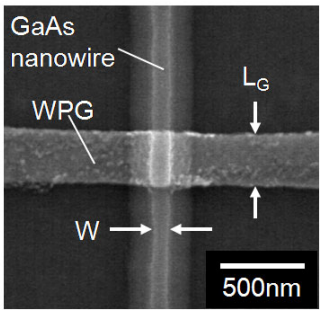

Fig. 2 SEM Image of fabricated a WPG QWRTr.

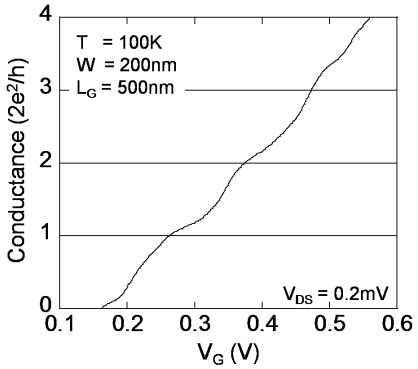

Fig. 3 Conductance characteristic at 100 K.

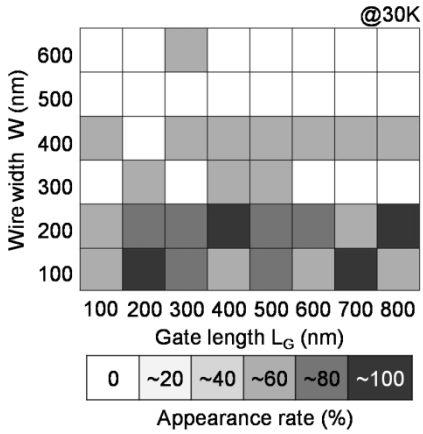

Fig. 4 Size dependence of appearance rate of conductance quantization at 30 K.

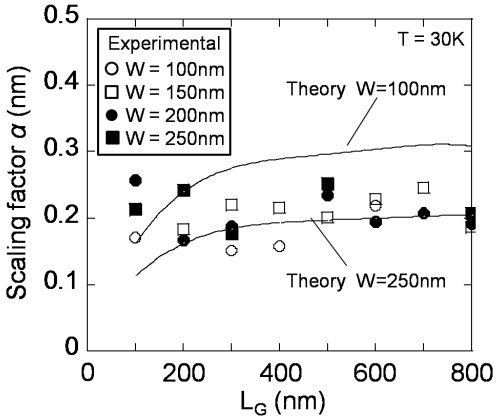

Fig. 5 Size dependence of V_G-to-E_F scaling factor.