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Fabrication of Two-Layer stacked Poly-Si TFT CMOS Inverters Using Laser Crystallized channel with metal gate on Si Substrate

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1. Introduction

In single Si layer ICs, the chip size is continually increasing despite reduction of feature size. Due to the scaling limit of VLSI technology, further increase of packing density or multiple functions will depend on the vertical integration technology. [1] It is considered that the structure of IC circuit consist of stacked active IC layers isolated by insulating materials. 3-D integration has several advantages such as high packing density, super large integration, high speed performance, parallel processing, integration of many functions on a single chip, and application of SOI technology etc.[2]

In this paper, we proposed two-layer poly-Si stacked CMOS inverters with PMOS TFT at upper poly-Si layer and NMOS TFT at lower poly-Si layer. Using laser crystallization techniques, the poly-Si channel with a high quality was obtained.

2. Experimental

Lower NMOS and upper PMOS TFT in 3-D stacked CMOS inverter were shown in Fig. 1. First layer of a-Si was deposited 100nm on SiO_2 layer by low pressure chemical vapor deposition (LPCVD). In order to fabricate the lower NMOS TFT of CMOS inverters, the crystallization of a-Si layer was performed with 400 mJ/cm^2 energy density using the KrF ELA system and 900mJ/ cm^2 using SLS method. Active area of NMOS was defined. After thermal growth of gate oxide with 8 nm and deposition of poly-Si gate, the source/drain (S/D) area was formed by phosphorus plasma doping at 450 ^{o}C to avoid the activation anneal at high temperature.[3] The deposition of interlayer dielectric (ILD) film to isolate the upper PMOS TFT from the lower NMOS TFT. Then, second layer of a-Si was deposited 100nm on the ILD and the crystallization of upper PMOS TFT was carried out by SLS laser annealing with 900 mJ/cm^2 energy density. After deposition high-k gate dielectric and Pt gate electrode, the S/D area of PMOS TFT was formed by boron plasma doping at 400 ^{o}C. The contact holes were opened at the S/D and gate of the lower NMOS TFT, and then the metallization.

3. Results and discussion

Figure 2 shows the X-ray intensity of poly-Si annealed by ELA with 400 mJ/cm^2 and SLS with 900 mJ/cm^2. The crystallized films showed preferred crystal orientations of (111), (220), and (311) directions. The crystallinity of both poly-Si films is considered to be adequate for poly-Si stacked TFT CMOS inverters.

Figure 3 shows the top-view of the SEM images of poly-Si film after etching of grain boundary using Secco etchant. The samples were crystallized by ELA with the laser energy density of 400 mJ/cm^2. The poly-Si film was uniformly crystallized and the average grain size was about 100nm. On the other hands, the poly-Si film by SLS technology with the laser energy density of 900 mJ/cm^2 was un-uniformly crystallized but the average grain size was larger than 100 nm. However, both poly-Si films of the average grain size were good enough for the TFT devices.

Figure 4 shows the atomic force microscope (AFM) images of laser crystallized poly-Si film. The surface roughness of ELA crystallized poly-Si film is relatively smooth and the RMS roughness is about 1.6 nm as shown in Fig. 4(a). On the other hand, the RMS roughness of SLS crystallized poly-Si film is about 2.88 nm as shown in Fig. 4(b). The RMS roughness on both ELA and SLS crystallized poly-Si grains were about 0.151nm. So such a smooth surface like single crystal was favorable for obtaining good performance TFTs. It is also considered that the poly-Si films by laser crystallization were good for poly-Si stacked TFT CMOS inverters.

Figure 5 shows the I_d - V_g characteristics of NMOS TFT and PMOS TFT with channel width/gate length, W/L=10 um/10 um. The maximum/minimum current ratio, sub-threshold swing of the NMOS TFT at lower poly-Si were about 10^7, 77mV/dec. with ELA(Fig 5(a)) and 10^7, 78mV/dec., respectively with ELA(b). On the other hand, the upper PMOS TFT was about 10^6, 135mV/dec. respectively. From these results, the electrical characteristics of both TFTs are comparable to those of bulk or SOI MOSFET and are attributed to the high quality crystallinity of laser annealed poly-Si films. Particularly, the sub-threshold swing of NMOS was remarkable for the TFT CMOS devices.

Figure 6 represents the DC voltage transfer characteristics (VTC) and the gain of the stacked CMOS inverter as a function of supply voltage from 1 V to 2.5 V of V_{dd} with

0.5V step, and V_{ss} = 0 V. As observed, the maximum gain equals 9, 13, 18, and 20 were measured from the slope of the voltage transfer curve in the transition region at 1V, 1.5 V, 2 V, and 2.5 V of V_{dd}. for the lower NMOS with ELA and upper PMOS with SLS. However, the maximum gain equals 2.3, 3.8, 5.5, and 8 were observed both the lower NMOS and upper PMOS with SLS. The output characteristics show abrupt transition at both high and low power supply.

4. Conclusions

We have successfully realized the 3-D stacked CMOS inverters with two-layer poly-Si TFTs that applicable to the high performance logic circuits. The grains of laser crystallized poly-Si films were uniforms and low RMS roughness. The poly-Si stacked TFT CMOS inverter revealed excellent output characteristics including DC voltage transfer characteristics for the 3-D vertical integrated CMOS applications. We verified the feasibility of 3-D stacked CMOS inverter circuit by poly-Si TFT technology.

References

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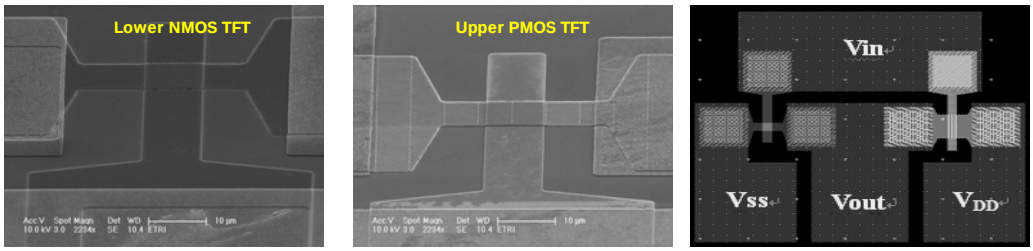


(a) (b) (c)

Figure 1. Top-view images of the fabricated 3-D stacked poly-Si CMOS inverter.(a) lower NMOS, (b) upper PMOS TFT in 3D stacked CMOS inverter (c) with channel width/gate length, W/L=10 um/10 um.

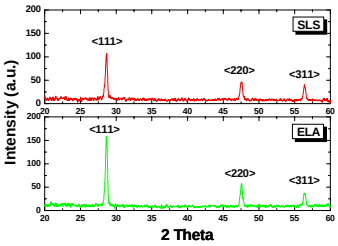
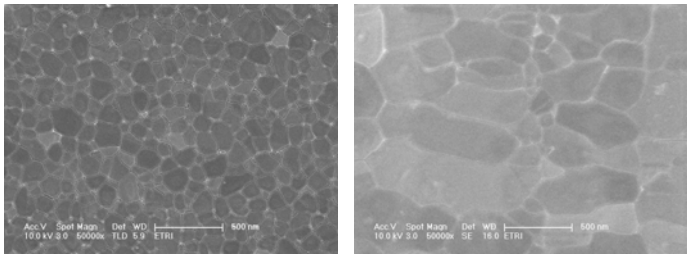
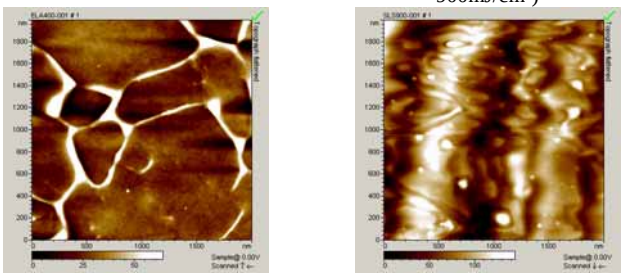


Fig. 2. X-ray Diffractometer of the laser anneal crystallized poly-Si film by ELA(E = 400mJ/cm^2), SLS(E = 900mJ/cm^2)



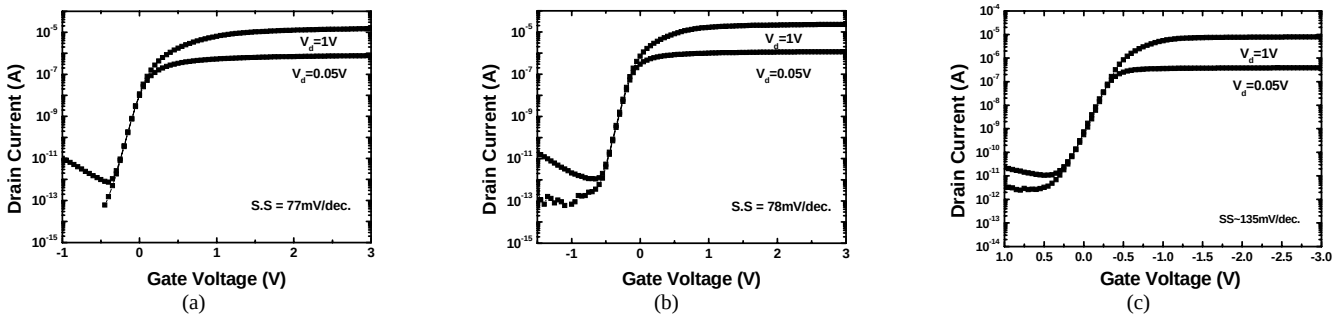
(a) (a)

Fig. 3. Top-view of SEM images after Secco etching of laser anneal crystallized poly-Si film by (a) ELA(E = 400mJ/cm^2), (b) SLS(E = 900mJ/cm^2).



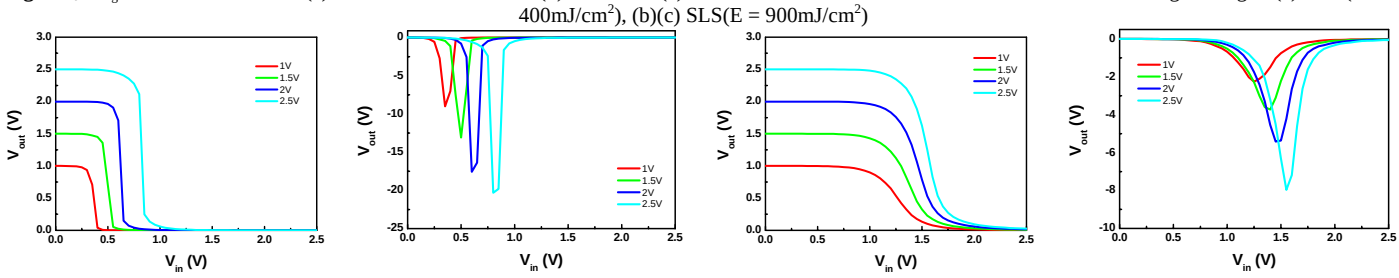
(a) (b)

Fig. 4. AFM images after Secco etching of laser anneal crystallized poly-Si film by (a) ELA(E = 400mJ/cm^2), (b) SLS(E = 900mJ/cm^2).



(a) (b) (c)

Fig. 5. I_d –V_g characteristics of the (a) NMOS TFT with ELA, (b) with SLS, (c) PMOS TFT with SLS of the CMOS inverter with 10um gate length. (a) ELA(E = 400mJ/cm^2), (b)(c) SLS(E = 900mJ/cm^2)



(a) (b) (c) (d)

Fig. 6. DC voltage transfer characterisitics and the gain of the CMOS inverter (W/L=10um/10um CMOS) (a)(b) lower NMOS with ELA and upper PMOS with SLS, (c)(d) lower NMOS and upper PMOS with SLS.