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Overview and Future Challenges of Floating Body RAM Technologies

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1. Introduction

A single transistor DRAM cell, which is generally called Floating Body Cell (FBC), makes use of its floating body formed on an SOI as a data storage node. One of the growing interests is its scalability to the future generations. This paper reviews operations of FBCs [1-13] and their relatives [14,15]. Scalability of an FBC estimated by device simulation and experimental results are demonstrated with emphasis on challenging issues.

2. Operation

Fig.1 explains a write operation of an FBC [1,2]. In the case of a fully-depleted (FD) FBC [3], a negative bias is applied to the plate (PL) so that an accumulation layer is formed at the back surface of an SOI film. Holes are stored at and extracted from this accumulation layer. To write "1" data, impact ionization is induced and holes are accumulated in the body. To write "0" data, a negative voltage is applied to the bit-line (BL). Holes are annihilated at the forward-biased pn-junction. By applying 0V to the BL and by applying a negative voltage to the word-line (WL), the body potential level is held for a certain time. The data states can be identified using MOSFET current modulated by the body potential level.

Variations of the write operation have been reported as listed in Table I. Writing "1" data can be performed by the Gate-Induced Drain Leakage (GIDL) current [5,6]. To write "0" data, a source-drain voltage is applied, and it is effectively assisted by over-driving the WL [4] and by driving the back word-line (BWL) [3]. Although some of these variations yield potentially larger signal margin, the write operation after Ref. [1,2] has been often studied due to the simple waveform and the small number of wirings to drive. Fig. 2 shows a waveform of operation after Ref. [2]. The body potential for "0"-cell and "1"-cell is also shown.

In terms of scaling, a partially-depleted device is less preferable because V_T fluctuation and junction leakage may be increased due to high doping concentration. In order to investigate scalability of an FD-FBC, device simulation has been carried out and the results are summarized in Table II [11]. The boundary condition for this study is to keep the threshold voltage difference (ΔV_T) and the retention time constant. For estimating the retention time, the maximum electric field in the "0"-hold cell (Emax) was used as a metric. Using the waveform in Fig.2, the ΔV_T and the Emax were calculated and the optimum structure and operation voltages of the FBC for the coming generations have been found. Keeping a ΔV_T of 0.4V and an Emax of 0.7 MV/cm, the FBC is scalable from the 90nm node to the 32nm node.

The refresh operation is possibly power-consuming. In some cases, a negative voltage is applied to the WL to cut off MOSFET current in the write operation [5,6,8]. A block refresh concept has been proposed [13] in which all cells are refreshed without having to read the data states of each cell.

3. Device Structure and Process Integration

To verify feasibility of the FBC for embedded memory applications, the 128Mb FBRAM have been fabricated using 90nm CMOS technology [10,11]. Fig.3 shows a device structure of the FBRAM. In order to increase the signal margin, the silicon film thickness of array device is smaller than that of peripheral device. Since an SOI wafer with thin buried oxide is used for the FBRAM, the cell structure and fabrication process are so simple that its cell size is shrinkable. A bulk-FBC [8] and a fin-FBC [9,12] have been proposed and developed. These approaches [8-12] provide potential FBRAM structures to realize low cost process integration while keeping performance of logic devices.

4. Signal Margin

Fig. 4 shows V_T distributions of 1Kb transistors of the FBRAM. A ΔV_T of 0.42V has been obtained. Standard deviations of V_T are less than 40mV. In order to enlarge the worst bit-to-bit separation, the ratio of the ΔV_T over the V_T variation ($\sigma_{VT0} + \sigma_{VT1}$) should be increased. It should be noted that the number of holes stored in the body is rather small in the coming generations as shown in Table II. Just like the conventional SRAM cells, variability control is very important for the FBCs.

5. Data Retention Time

Measured data retention time of the FBRAM is 50μs at –4.6σ and 70ms at 0σ [11]. The retention time gives a great impact on the refresh power. Careful design and processing to reduce the Emax and traps are required for the FBCs. The issues are common to the conventional DRAM array devices.

6. Conclusion

Ideas and technologies of the FBCs have been evolved and crystallized as a memory. Combining unique features of the FBCs with design methodology of the conventional memory devices, we'll find answers to the challenging issues.

References

[1] S.Okhonin, *et al.*, *IEEE Int. SOI Conf.*, 2001, pp.153-154.
[2] T. Ohsawa, *et al.*, *Proc. ISSCC*, 2002, pp.152-153.
[3] C. Kuo, *et al.*, *IEDM Tech. Dig.*, 2002, pp843-846.
[4] P. C. Fazan, *et al.*, *CICC*, 2002, pp.99-102.
[5] P. Fazan, *et al.*, *ISDRS*, 2003, pp.386-387.
[6] E. Yoshida, *et al.*, *IEDM Tech. Dig.*, 2003, pp.913-916.
[7] R. Ranica, *et al.*, *IEDM Tech. Dig.*, 2004, pp.277-280.
[8] R. Ranica, *et al.*, *Symp. VLSI Tech. Dig.*, 2005, pp.38-39.
[9] S. Okhonin, *et al.*, *ICMTD*, 2005, pp.63-65.
[10] Y. Minami, *et al.*, *IEDM Tech. Dig.*, 2005, pp.317-320.
[11] T. Shino, *et al.*, *IEDM Tech. Dig.*, 2006, pp.569-572.
[12] I. Ban, *et al.*, *IEDM Tech. Dig.*, 2006, pp.573-576.
[13] P. Fazan, *et al.*, *IEEE Int. SOI Conf.*, 2003, pp.15-16.
[14] F. Morishita, *et al.*, *CICC*, 2005, pp.435-438.
[15] H. J. Cho, *et al.*, *IEDM Tech. Dig.*, 2005, pp.321-324.

Table II Scalability of FBC predicted by simulation.

	Generation	90nm	65nm	45nm	32nm
Structure	Cell Size (μm2)	0.1372	0.068	0.0336	0.02035
	Tsi (nm)	42	32	21	16
	Body Conc (cm-3)	3E17	2E17	1E17	1E17
	Tbox (nm)	25	17	12.5	9
	Lg (nm)	150	110	75	55
	Tox (nm)	6.0	5.6	5.2	4.8
Bias	Vwlh (V)	1.5	1.35	1.2	1.0
	Vwll (V)	–2.3	–2.0	–1.7	–1.45
	Vblh(V)	2.2	1.9	1.7	1.5
	Vbll (V)	–1.5	–1.2	–0.9	–0.7
	Vpl (V)	–3.0	–2.7	–2.4	–2.1
Results	Vth1 (V)	0.327	0.271	0.277	0.327
	Vth0 (V)	0.724	0.671	0.674	0.695
	δVth (V)	0.397	0.400	0.397	0.368
	"1" Cell Hole Number (/μm)	2613	2193	1447	1028
	"0" Cell Hole Number (/μm)	165	75	12	6.8
	Emax (MV/cm)	0.72	0.70	0.70	0.74

Table I Bias conditions in write operation.

Ref.	"1" write	Vg	Vs	Vd	Vp	"0" write	Vg	Vs	Vd	Vp	Wirings to drive
[1][2]	I/I	++	Gnd	+++	-	FB	++	Gnd	-	-	BL, WL
[1]	I/I	-	Gnd	--	-	FB	++	Gnd	-	-	BL, WL
[3]	I/I	++	Gnd	+++	-	FB	++	Gnd	+	+	BL, WL, SL, BWL
[4]	I/I	+	Gnd	++	-	FB	+++	Gnd	++	-	BL, WL
[5]	GIDL	-	Gnd	+	-	FB	-	Gnd	-	-	BL, WL
[6]	GIDL	-	Gnd	+	-	FB	++	Gnd	-	-	BL, WL
[7]	I/I	++	Gnd	+++	-	FB	++	Gnd	+	+	BL, WL, BWL
[8]	I/I	++	Gnd	+++		FB	-	-	Gnd		BL, WL, SL

I/I:Impact Ionization, FB:Forward Biasing, Vg: WL, Vs: SL, Vd: BL, Vp: PL(BWL)

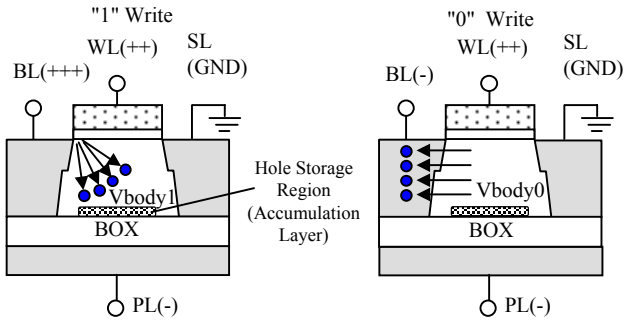

Fig.1 Write operation.

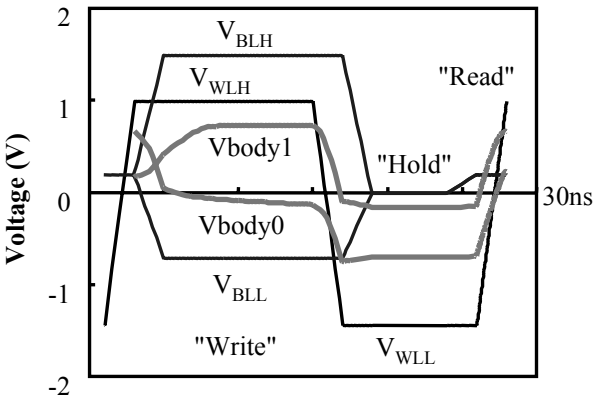

Fig.2 Waveform of operation after Ref.[2] (32nm node).

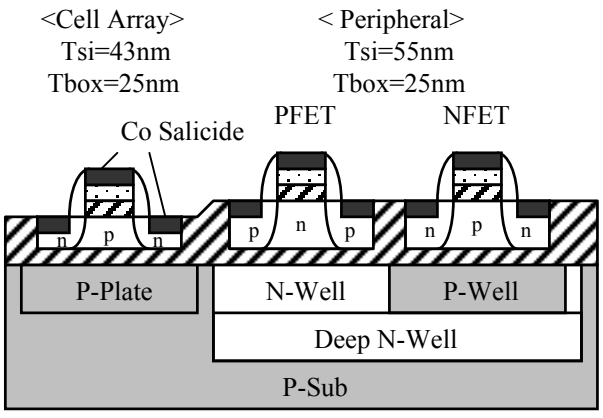

Fig.3 Device structure of FBRAM using FBC.

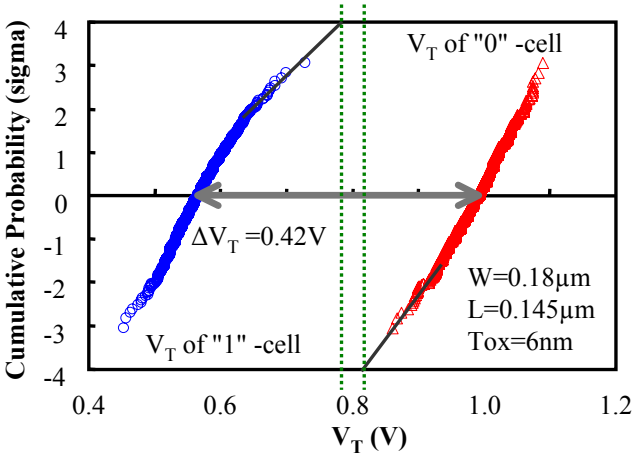

Fig.4 V_T distribution of FBC array of 1Kb.