

RC-FinFET (Recessed Channel FinFET) Cell Transistor Technology for Future Generation DRAMs

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1. Introduction

As the minimum feature size of a DRAM cell transistor scales down, the demand for large on-current and low off-state leakage current gets stronger to satisfy high-speed operation and good data retention characteristics. For conventional planar cell transistors, channel doping level has been continuously increased to suppress off-state leakage, which resulted in decrease of the retention time.

The Recess-Channel-Array Transistor (RCAT) and the Sphere-shaped-Recess-Channel-Array Transistor (SRCAT) had been proposed to control the short channel effect (SCE) by structural approach, that is by enlarging effective channel length, and had great achievements in improvement of cell data retention time (fig. 1) [1,2].

As a candidate for the future DRAM cell transistor, FinFET structure has great attraction because of its excellent gate controllability to suppress SCE and large current drivability coming from large effective channel width and small body bias effect [3]. In spite of these advantages, due to its low doping concentration in fully depleted thin body region, an *in situ* boron doped poly-silicon gate (p+ poly gate) is mandatory for suppression of the off-state leakage current to adjust threshold voltage (V_{th}) and to avoid increase of negative word-line voltage. With a p+ poly gate, a local damascene FinFET DRAM (LD-FinFET) scheme to prevent passing gate noise effect on storage node junctions of adjacent access cells was successfully integrated [4].

2. Device Design and Fabrication

As a cell gate spacer becomes shorter with scale down, junction electric field gets stronger because of an abrupt impurity profile formed by diffusion from highly doped plug pad poly-silicon. In order to reduce GIDL current induced by high electric field, a broad junction profile is indispensable. However, it makes the effective channel length shorten and deteriorates the SCE of the device. Fig. 2 shows the co-relation of off-state current (I_{off}) and GIDL of LD-FinFETs. There is very small room to improve both GIDL and SCE simultaneously even with a FinFET structure.

To solve this problem, we applied a recessed channel to an LD-FinFET that enlarges the device design window to improve static retention time (GIDL) and dynamic retention time (I_{off}). Fig. 3 shows the structures of an RC-FinFET with 80nm design rule DRAM cell. After STI CMP and local damascene processes [4], field oxide is etched away with a photo resist mask, and then remained SiN on channel regions and channel region silicon is removed sequentially. For an RC-FinFET structure, we need only three additional steps compared to an LD-FinFET: SiN etch-back, silicon recess, and wet etch to round a recessed region. The recessed silicon depth is 50nm and recessed field oxide is 170nm, that is, fin height is 120nm. The fin width is 35nm at fin top region. A passing gate effect can be suppressed by adopting the local damascene scheme. There is no difference the other process conditions including junction and channel implantation conditions between an LD-FinFET and an RC-FinFET.

3. Results

Current drivability comparison between the LD-FinFET and the RC-FinFET is shown in figs. 4 and 5. Cell on-currents at the same gate over-drive and $V_{ds}=1.2V$ are 19.5uA for an RCAT, 32.5uA for an LD-FinFET, and 32.2uA for an RC-FinFET, respectively. Due to relatively long effective channel length and low electron mobility along a complex crystal plane, drain current of an RC-FinFET is smaller than LD-FinFET about 5% at the same gate over-drive voltage and high drain bias. However, this difference can be negligible at cell operational voltage and an RC-FinFET still has much large on-current compared to an RCAT.

Figs. 6, 7 and 8 show the body bias effect (BBE) of V_{th} , drain induced barrier lowering effect (DIBL), and sub-threshold swing (SS) characteristics, respectively. BBE and SS of an RC-FinFET are similar to those of an LD-FinFET, while DIBL of an RC-FinFET is much smaller than that of an LD-FinFET. Both structures have better short channel immunity compared to an RCAT. High current drivability and small BBE could make it possible to lower word-line boost voltage V_{pp} which is given by $V_{pp} > V_{th} + V_{cc} + BBE$ and to reduce a reliability burden of V_{pp} node support transistors.

I_{off} of an RC-FinFET is reduced compared to an LD-FinFET at the same GIDL as shown in fig. 9. This fact means that it is possible to reduce GIDL to obtain sufficient static retention time by using more graded junction profile without increase of I_{off} and degrade of dynamic retention time. V_{th} of an RC-FinFET could be reduced compared to an RCAT for its small SS, namely, an RC-FinFET cell has the same level of a dynamic retention margin with about 150mV lower V_{th} than an RCAT (fig. 10). Data retention characteristics of an LD-FinFET and an RC-FinFET are compared in fig. 11, which shows that retention time of an RC-FinFET is improve about 55% than that of an LD-FinFET at the given fail bit criteria.

4. Conclusion

An RC-FinFET (Recessed Channel FinFET) cell transistor has been successfully integrated in DRAM. An RC-FinFET has better SCE immunity and can be optimized to have lower GIDL relative to a conventional LD-FinFET. This fact leads an RC-FinFET has about 55% longer static retention time than an LD-FinFET.

References

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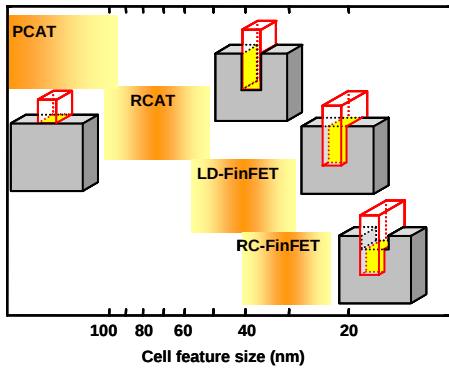


Fig. 1 Structure progress of DRAM cell transistors.

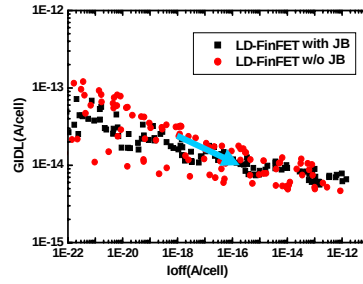


Fig. 2 GIDL-Ioff correlation with and without junction broadening (JB). Junction broadening makes GIDL makes small but SCE becomes worse.

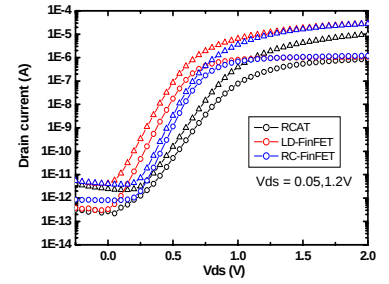


Fig. 4 Id-Vg characteristics. RC-FinFET shows the most excellent SCE controllability.

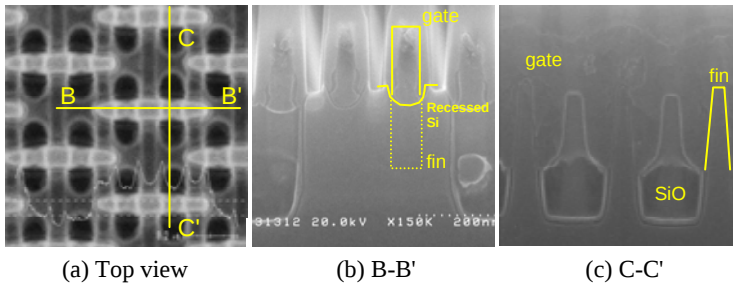


Fig. 3. Structure of fabricated devices. (a) top view after recess formation, (b) vertical image perpendicular to word-line direction, (c) vertical image parallel to word-line direction.

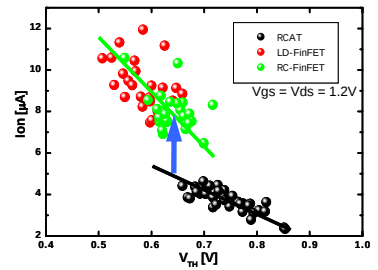


Fig. 5 Comparison of V_{th} vs Ion correlation. Ion of RC-FinFET is about 60% larger than RCAT.

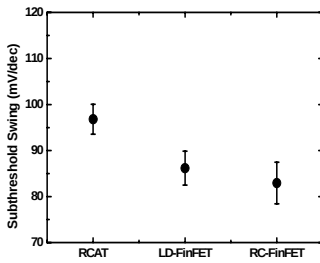


Fig. 6. Comparison of Subthreshold swing (SS) at 85C. RC-FinFET has nearly ideal SS characteristics.

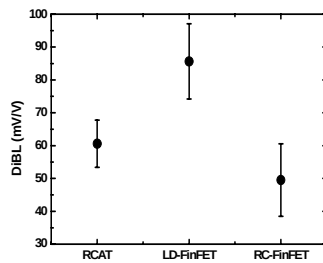


Fig. 7. DIBL of three different structures. RC-FinFET has small DIBL and more room to optimize GIDL without degradation of SCE.

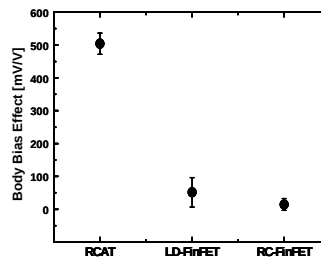


Fig. 8. Body bias effect (BBE) of V_{th} . BBE of FinFET is negligibly small. Small BBE of FinFETs could make it possible to lower word-line boost voltage.

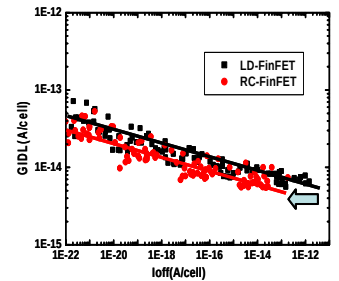


Fig. 9. GIDL-Ioff correlation. GIDL of RC-FinFET is about 50% smaller than LD-FinFET at the same Ioff.

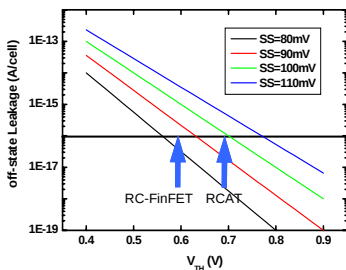


Fig. 10 Allowed threshold voltage to satisfy critical off-state leakage current and dynamic refresh time with various SS.

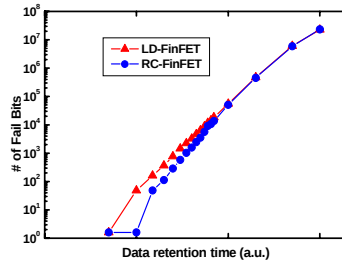


Fig. 11. Data retention characteristics of LD-FinFET and RC-FinFET at 85C.

Table 1. Characteristics comparison

	RCAT	LD-FinFET	RC-FinFET
Ion(uA)	9.5	32.5	32.2
DIBL(mV/V)	60.5	85.6	49.5
SS(mV/dec)	97	86	82
BBE(mV/V)	500	51	14