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Self-aligned Fabrication Process for Pd-Contacted and PMMA-Passivated Carbon Nanotube Field-Effect Transistors

Lorraine Rispal, Hongyu Yang, Rudolf Heller, Gisela Hess, Gerhard Tzschöckel, Udo Schwalke

Institute for Semiconductor Technology, Darmstadt University of Technology
Schlossgartenstrasse 8, D-64289 Darmstadt, Germany
Phone: +49 6151 164471 Fax : +49 6151 165233 E-mail: rispal@iht.tu-darmstadt.de

1. Introduction

Since 1998, many groups of researchers tried to fabricate transistors where carbon nanotubes (CNTs) act as the channel. Two main processes are used: separate growth of SWNTs (Single-walled CNTs) usually by laser ablation and dispersion from a solvent by spinning onto the silicon wafer [1], or in-situ growth of the SWNTs directly on the wafer with chemical vapor deposition (CVD) [2]. In this work, we present a novel process to fabricate carbon nanotube field-effect transistors (CNTFETs). It is based on CVD growth of CNTs using a 'sacrificial' catalyst. The SWNTs are grown uniformly across the wafer surface and subsequently contacted with palladium and passivated with PMMA in one step. The process contains neither complicated manipulations of the SWNTs nor multi-step lithography, avoiding the risk of misalignment. We choose the in-situ growth method because it looks the most practical for future use in microelectronics where millions of transistors need to be fabricated at the same time.

2. Experimental

Highly doped p-type silicon wafers are first oxidized (40 nm SiO_2) in order to isolate the SWNTs from the gate electrode, i.e., the Si substrate. Then, a catalyst layer is evaporated to stimulate SWNT growth (0,5 nm Ni on 5 nm Al). Subsequently, the wafers are annealed to 870°C in a CVD reactor in N_2 at atmospheric pressure for 5 min to form Ni-nanoclusters, which act as catalyst particles for SWNT growth. Afterwards, SWNT growth occurs for 10 min in a CH_4/H_2 mixture at the same temperature in the same furnace uniformly across the surface of the wafer. During this high-temperature step and because of reaction with SiO_2, the thin 5 nm Al/ 0.5 nm Ni metal-catalyst converts into an Al_2O_3 film (high-k dielectric) covered with discontinuous Ni-nanoclusters (see Fig. 1 and 2). This kind of 'sacrificial' catalyst allows the gate field to penetrate and control the current flow within the SWNTs. Finally Pd source/drain (S/D) electrodes are patterned by photolithography and subsequent metal lift-off without the need of alignment. Pd has been used because its high work function is well-known to provide very good contacts to the SWNTs [3]. The photolithography has been realized with a special double layer resist (photoresist on PMMA). The PMMA is not photosensitive but is etched during development so that a small under-etching appears (see Fig. 1 left). We evaporate Pd while rotating the wafer chuck so that the metal covers the whole area under the photoresist (see Fig. 1 and Fig. 4 inset). To remove the resist, we use either traditional solvent for non-passivated devices (see Fig. 3 right) or special remover that did not solve PMMA for passivated CNTFETs (see Fig. 1 right and Fig. 4 inset). In our previous work [4], patterned Al/Ni catalytic areas could be directly used as S/D electrodes since conductive amorphous carbon covered them. This was due to CH_4 pyrolysis that occurred when no H_2 is mixed to CH_4 during the CVD process [5]. This previous self-aligned process gave also working transistors, but high contact resistances between electrodes and SWNTs imply high S/D voltages (30V).

3. Measurements and results

After fabrication is completed, the CNTFETs are measured using a semiconductor parameter analyzer. The density of SWNTs was adjusted so that only one nanotube bridges the electrodes on average, corresponding to a channel width of about 1 nm (average diameter of our SWNTs). The channel length is 2 µm. Passivated CNTFETs show improved characteristic in comparison with non-passivated ones (see Fig. 3 left and 4 for two typical examples of transfer characteristics). Non-passivated and passivated devices provide an on-current of about 2 µA (i.e. 2 mA/µm) at Vds of 400 mV and an on/off ratio of about 10^4 (Note that the off-current sensitivity is limited by the measurement set-up. Improved low noise probes should decrease the off-current from 200 pA to 2 pA so that the on/off ratio is expected to improve to 10^6). The slope and the hysteresis are smaller in passivated devices (respectively 180 mV/dec instead of 250 mV/dec and 570 mV instead of 750 mV). All the measurements presented in this paper have been executed in room conditions (44% humidity and 22°C). We believe that with more humidity, the hysteresis of non-passivated devices will increase because hysteresis is probably due to charge trapping by water molecules around the nanotubes [6]. Moreover, after two weeks, more than half of the non-passivated transistors do not work anymore whereas more than three quarter of the passivated devices are still fully functional.

Measurements on passivated CNTFETs have shown that there are three kinds of SWNTs forming the channel: about 55% show a pure semiconducting behavior (on/off ratio $\geq 10^4$, see Fig. 4 as an example of transfer characteristic on such a device), 30% are also semiconducting but with a small band-gap ("semi-metal" behavior with small on/off ratio, see Fig. 5 left as an example with on/off ratio of 6) and 15% are purely metallic (no field-effect notable,

see Fig. 5 right). This distribution corresponds approximately to the theory [7]. Lastly, some experiments on hysteresis revealed that it depends strongly on the cycling range of the gate voltage. Using Vg from -1V to 1V reduces considerably the hysteresis width but this is not enough to achieve the saturation off-current (see Fig. 6).

4. Conclusions

In conclusion, we have fabricated CNTFETs with a novel self-aligned CMOS-compatible process. The transistors are contacted with Pd and passivated with PMMA in one step lithography. They are PMOS-like CNTFETs with on/off ratios up to 10^4 and show improved characteristics (smaller slope and hysteresis, longer lifetime) in comparison with non-passivated ones. Further improvement of this fabrication method, like annealing after passivation [6], should lead to hysteresis-free transfer characteristic, essential prerequisite to the integration of CNTFETs in the CMOS technology. The excellent performance of the CNTFETs at the very low Vds of 400 mV make them suitable for ultra-low voltage low-power applications.

References

[1] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke and Ph. Avouris, Appl. Phys. Lett. **80** (2002), 3817.

[2] R. Seidel, M. Liebau, G. S. Duesberg, F. Kreupl, E. Unger, A. P. Graham and W. Hoenlein, Nanolett. **3** (2003) 965.

[3] A. Javey, J. Guo, Q. Wang, M. Lundstrom and H. Dai, Nature **424** (2003) 654.

[4] L. Rispal, Y. Stefanov, F. Wessely and U. Schwalke, Jpn. J. Appl. Phys. **45** (2006) 3672.

[5] N. R. Franklin, Y. Li, R. Chen, A. Javey and H. Dai, Appl. Phys. Lett. **79** (2001), 4571.

[6] W. Kim, A. Javey, O. Vermesh, Q. Wang, Y. Li and H. Dai, Nanolett. **3** (2003) 193.

[7] W. Kim, H. C. Choi, M. Shim, Y. Li, D. Wang and H. Dai, Nanolett. **2** (2002) 703.

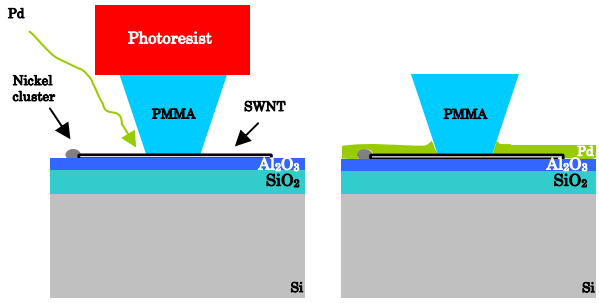

Fig. 1 Schematic of layer arrangement of CNTFETs. Left: during Pd-Evaporation. Right: final structure.

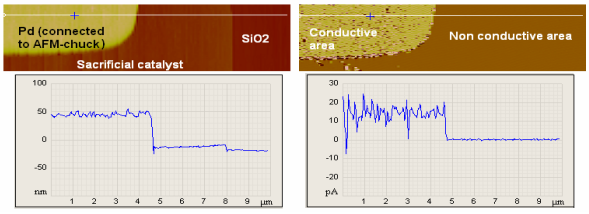

Fig. 2 Conductive AFM measurement of a test structure. Topographical scan (left) with height cross-section along the white line (left bottom): The step created by sacrificial Al/Ni catalyst is still visible. Electrical scan (right): Only Pd-electrode is visible. Both, sacrificial Al/Ni catalyst area and SiO_2 are non-conductive (see also [4] about the conductive-AFM measurement method).

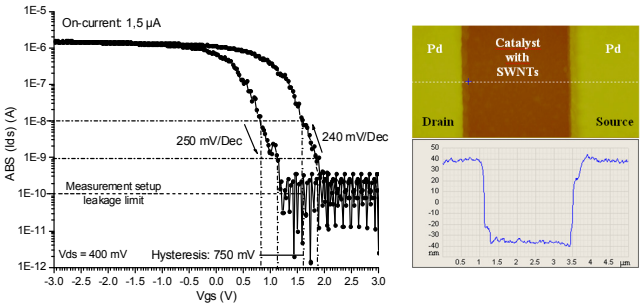

Fig. 3 Transfer characteristic of non-passivated CNTFET (left) and AFM topographical scan of the structure (right).

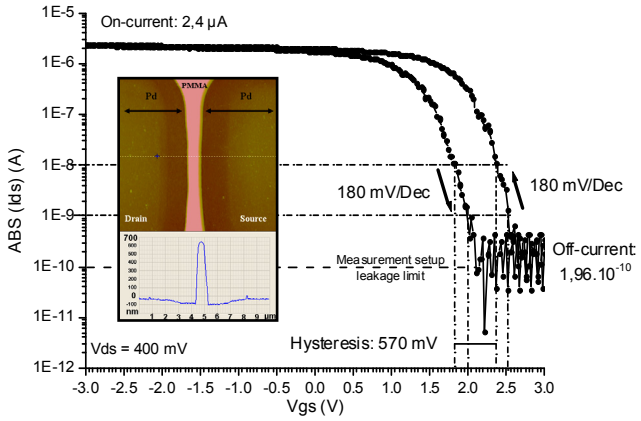

Fig. 4 Transfer characteristics of a semiconducting SWNT-FETs and AFM-topographical scan of the structure (inset).

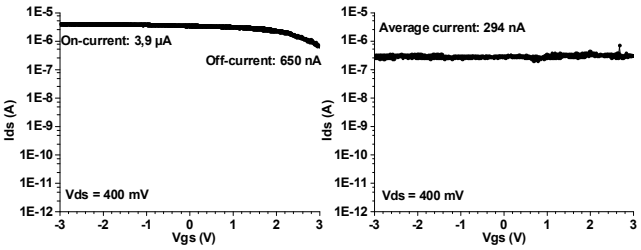

Fig. 5 Transfer characteristics of passivated CNTFETs: Small band-gap semiconducting SWNT-FET (left), "metallic SWNT-FET" (right).

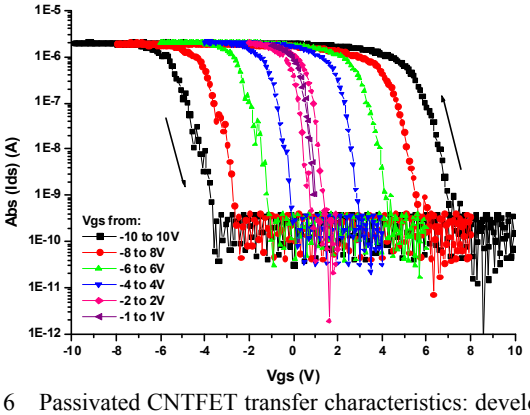

Fig. 6 Passivated CNTFET transfer characteristics: development of the hysteresis with increasing gate voltage cycling ranges.