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3D Device Stacking Technology for Future Memory

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I. Introduction

As the Si technologies advance to near 30nm dimensions, the conventional linear shrinkage of semiconductor devices can not keep up with the past trend at same speed due to the lithography and physical limitations. After the slowing down period in a scaling trend, finally, we will face ultimate physical limits of the Si device scaling and economic limits of the manufacturing due to ever-increasing fabrication cost for the scaling as shown in Fig.1.

For the physical limits the most widely predicted number is near 20nm because the transistor can still contain a few 10 electrons which is a minimum number to avoid noise errors from random telegraph noises and statistical fluctuation. However, the economical limits will come earlier than the physical limits. For example, below 35nm, current ArF lithography will not be usable anymore. Therefore, EUV, which has 13.5nm wavelength, is considered as a next generation lithography tool. The cost of EUV tool is much more expensive compared to ArF. In the memory technology, the continuous bit cost down with increasing the bit density is one of the most important factor to continue the business with proper profit as shown in Fig.2 . For example, as a simple way to increase the density in a given footprint, chips or packages have been stacked. However, the bit cost cannot be reduced by this method, because it is the only stacking of the fully integrated Si chips for increasing the bit density regardless of the total cost. By the 3D device staking technology in the memory, we can expect to meet both requirements of the bit cost down and the improvement in the performance simultaneously. Thus, device stacking is indispensable in memory.

In this paper, our examples of 3D device stacking in memory are presented and the key technologies for 3D device staking are briefly discussed.

II. Embodiment of 3D Device Stacking technology in Memory

The 3D device stacking technology in memory has begun recently with SRAM in order to reduce its large cell size and overcome the limits in its shrinkage. [1]. The area penalty of embedded SRAM cache in CPU chip reaches up to 80%. So, the need for a relatively cheap external cache memory is growing. But, typical 6T full CMOS SRAM cell size of ~$84F^2$ is too large to get an appropriate high density SRAM. Moreover, the simple linear shrinkage is not so easy in SRAM due to well-to-well isolation and too many contact holes and local interconnections. By implementing of our double stack technology, the load PMOS and the access NMOS are stacked up on the 2nd and 3rd device layers respectively over the 1st bulk pull-down NMOS, we have achieved an extremely small SRAM cell of $25F^2$ and the well isolation limit has been fundamentally eliminated as shown in Fig.3. By mixing the device stacking technology and a chip stacking technology, it is possible to make a high performance CPU chip in the near future by the coupling of a core only chip and the 3D device stacked SRAM cache

As for NAND flash memory, the linear shrink is already near in the ultimate limit regarding to the bit cost down and the fundamental reliability issues originated from very small feature size below 35nm. Thus, the application of the 3D device stacking technology to NAND flash is very imminent. The successful implementation of 3D device stacking technology into the double stacked SRAM has encouraged us to pursue the stack NAND flash and we have recently succeeded in the chip level function.[2] The device stacking technology in NAND flash is much different from concepts in the SRAM. The cell arrays are on the 2nd or 3rd Si layers stacked with exact copying of the 1st layer cell array patterns as shown in fig. 4. Then, the entire cell array and peripheral circuits is interconnected simultaneously with same interconnection layers such as bit line, common source line, and metallization layers. This cell array stacking method can reduce the bit cost with increasing the bit density.

III. Key Technologies in 3D Device Stacking for Memory

i. Formation of Single Crystal Si Layer on ILD

The formation of perfect SOI-like single crystal silicon layer on ILD (Inter Layer Dielectrics) layers is the most crucial process in the device stacking because the performance of the upper layer device should be same with it of the silicon bulk device. There are several known methods to obtain single crystal silicon layer on ILD, such as epitaxy lateral overgrowth, selective epitaxial deposition + lateral solid phase epitaxy, and selective epitaxial deposition + laser epitaxial growth as shown in Fig.5. Essentially, all of the processes use the single crystal silicon of the lower(bulk) layer as a seed. Even though it seems that the processes must be further improved and optimized, we can say that the real product level is not in the distant future.

ii. Multilayer Contact with Very High Aspect Ratio

As the second device layer is stacked on ILD, the depth of necessary contact becomes deeper and the contact has to connect multilayer between 1st and 2nd device layers. Moreover, the critical dimension of the contact gets smaller. Thus, the formation of the contact in the 3D device stacking is another challenging issue.

iii. Low Thermal Process

In order to minimize an adverse effect on the device of the lower layer, an additional thermal budget should be minimized during the device fabrication of the upper layer. However, there is a trade-off between the thermal budget and the reliability characteristics of dielectric layers. New concepts, new materials and novel integration methods are needed to facilitate the 3D device-staked memory.

Conclusions

When the linear shrinkage of the planar CMOS technology reaches to the fundamental limit, the 3D stacking technology seems to be the only solution. In addition to cost effectiveness, the advantages of stacking devices are numerous. By stacking the various functional devices in the near future, a totally innovative product with sophisticated multi-functional electronics will be developed. Thus, 3D device stacking technology will be quickly established in field of memory and logic product for achieving better performance and cost effectiveness.

References

[1] Soon-Moon Jung, et al.: Tech. Dig. VSLI'04, pp.265, 2004

[2] Soon-Moon Jung, et al.: Tech. Dig. IEDM'06, pp.37,2006

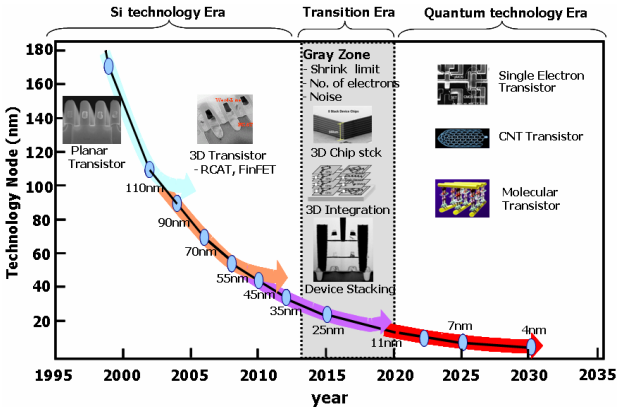


Fig.1 The past trends and prospects on silicon technology.

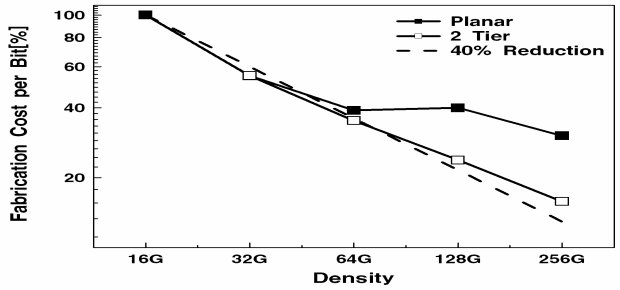


Fig. 2 Predictions of fabrication cost of NAND flash memory as the bit density increases

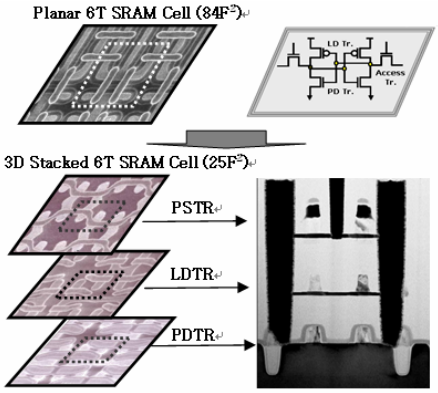
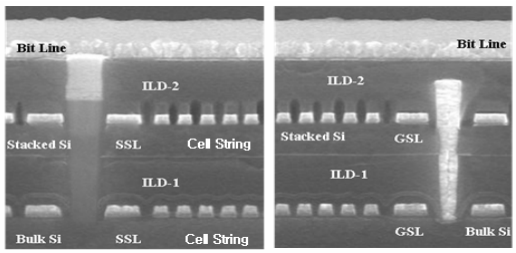


Fig.3 3-D integration technology for SRAM cell . The cell size can be reduced dramatically to 25 F^2 from 84 F^2 of planar 6T .



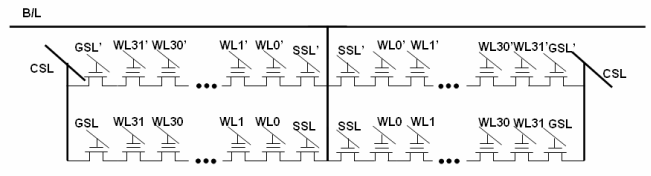
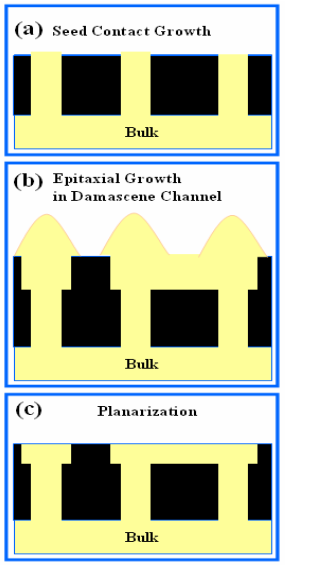


Fig.4 Double-stacked TANOS cell arrays in CT-NAND



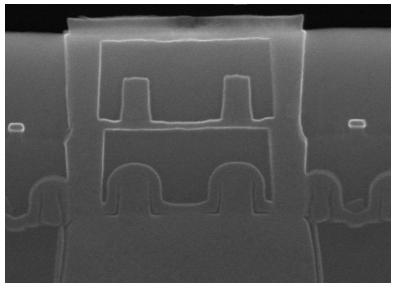


Fig.5 Vertical Schematics of the formation of single-crystalline Si layer on ILD

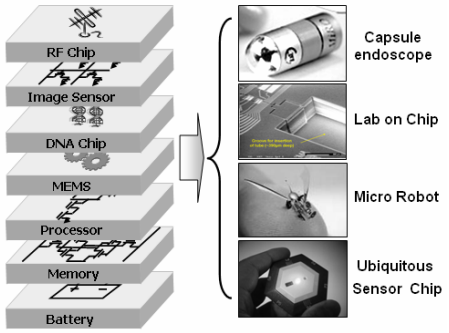


Fig.6 A schematic illustration of multi function electronics by 3D integration of either heterogeneous materials or differently functioning devices